

APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	304 S/P

FIG. 1

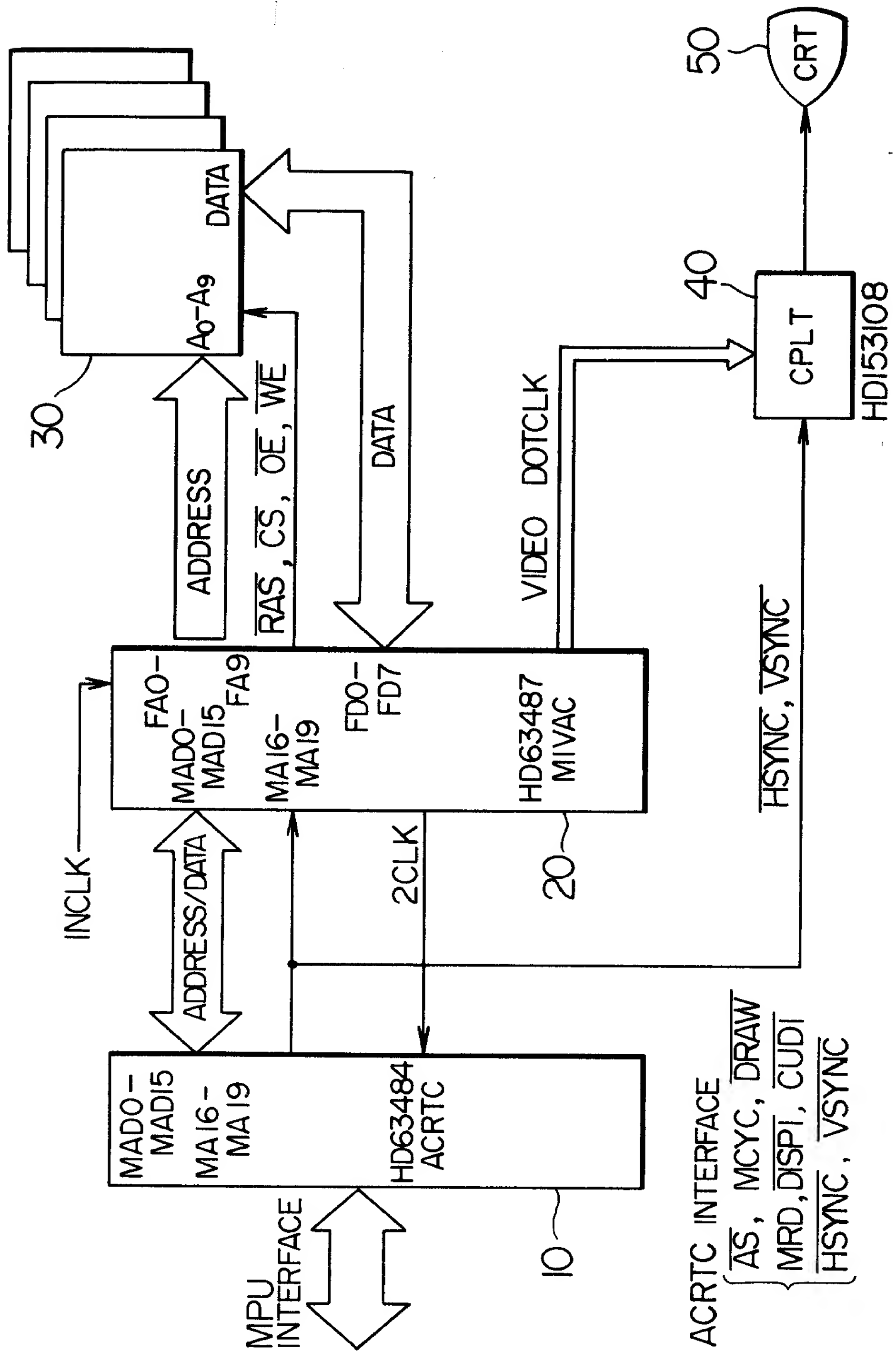


FIG. 2

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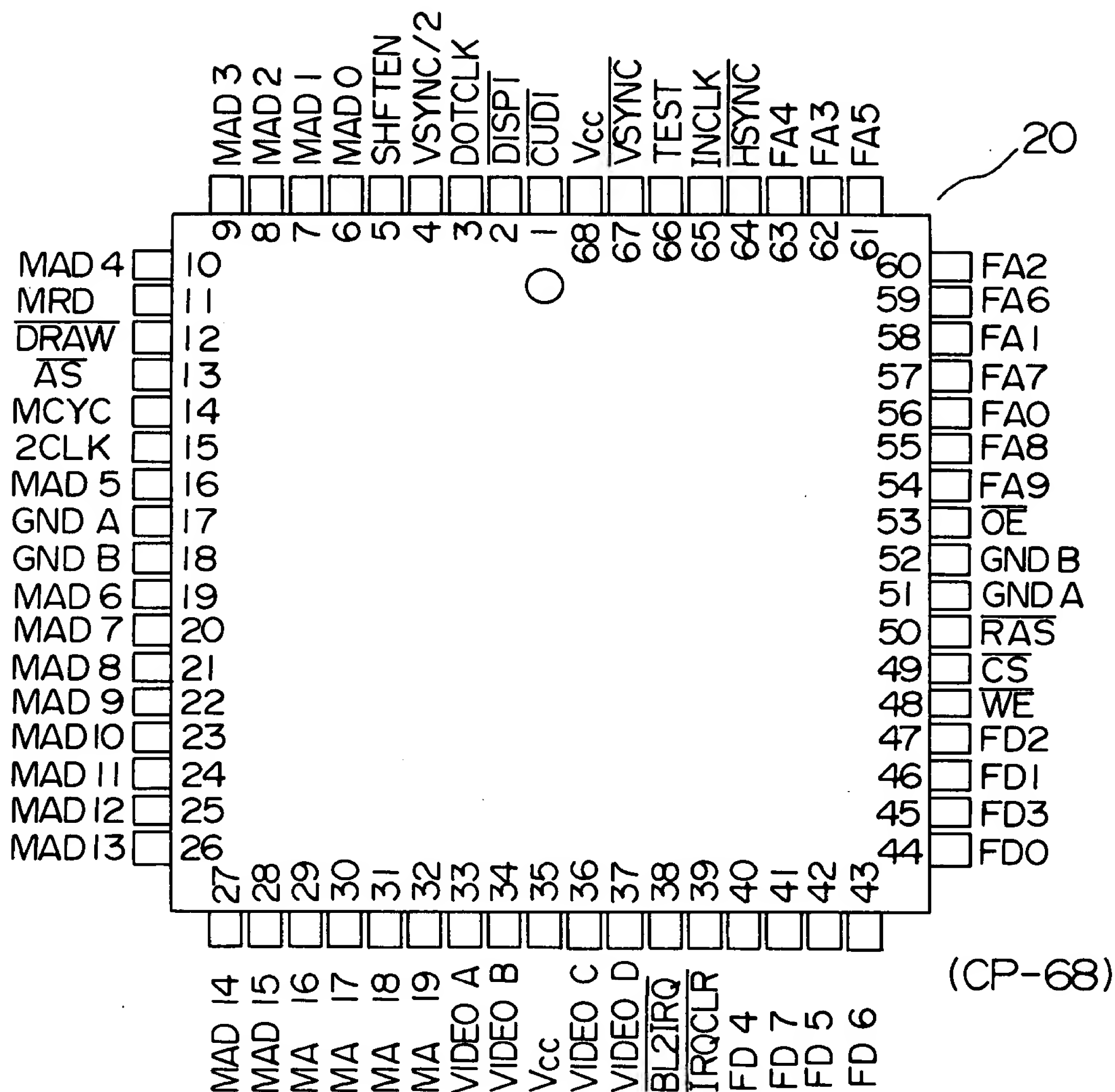


FIG. 3a

ITEM	TERMI- NAL NO.	TERMI- NAL NAME	INPUT/ OUTPUT	FUNCTION
POWER SUPPLY	35, 68	Vcc	—	+ 5V IS SUPPLIED.
	17, 18 51, 52	Vcc	—	GND IS CONNECTED.
OPERATION CONTROL SIGNAL	65	INCLK	INPUT	BASIC CLOCK OF MIVAC IS INPUTTED.
	66	TEST	INPUT	MIVAC OPERATION IS TESTED. SET THIS TERMINAL TO "LOW" LEVEL.
ACRTC INTERFACE SIGNAL	15	2CLK	OUTPUT	2CLK SIGNAL IS SUPPLIED TO ACRTC. THIS SIGNAL IS ASYMMETRIC, NAMELY, HAS DIFFERENT CYCLE LENGTHS IN THE FIRST HALF AND SECOND HALF OF A MEMORY CYCLE.
	14	MCYC	INPUT	MCYC SIGNAL FROM ACRTC IS INPUTTED. MCY0 INDICATES "LOW" AND "HIGH" LEVELS WHEN ACRTC IS IN ADDRESS AND DATA CYCLES, RESPECTIVELY.
	12	$\overline{\text{DRAW}}$	INPUT	$\overline{\text{DRAW}}$ SIGNAL FROM ACRTC IS INPUTTED. $\overline{\text{DRAW}}$ INDICATES WHETHER OR NOT ACRTC IS IN THE DRAW CYCLE. $\overline{\text{DRAW}}$ IS "LOW" LEVEL IN THE DRAW CYCLE AND IS "HIGH" LEVEL IN THE OTHER CYCLES.
	11	MRD	INPUT	MRD SIGNAL FROM ACRTC IS INPUTTED. MRD CONTROLS DATA TRANSFER DIRECTION BETWEEN FRAME BUFFER AND ACRTC. WHEN DATA IS READ FROM FRAME BUFFER, "HIGH" LEVEL IS INPUTTED. WHEN DATA IS WRITTEN IN FRAME BUFFER, "LOW" LEVEL IS INPUTTED.
	13	$\overline{\text{AS}}$	INPUT	$\overline{\text{AS}}$ SIGNAL IS INPUTTED FROM ACRTC. $\overline{\text{AS}}$ INDICATES PRESENCE OR ABSENCE OF MEMORY ACCESS.
	64	$\overline{\text{HSYNC}}$	INPUT	$\overline{\text{HSYNC}}$ SIGNAL IS INPUTTED FROM ACRTC. UNDER CONDITIONS OF $\overline{\text{HSYNC}}$ = "LOW" AND $\overline{\text{DRAW}}$ = "HIGH", IF AS PULSE IS RECEIVED, $\overline{\text{CS}}$ BEFORE RAS REFRESH OPERATION IS CARRIED OUT.
	67	$\overline{\text{VSYNC}}$	INPUT	$\overline{\text{VSYNC}}$ SIGNAL IS INPUTTED FROM ACRTC. RECEIVED $\overline{\text{VSYNC}}$ IS DIVIDED BY TWO SO AS TO OUTPUTTED AS $\overline{\text{VSYNC}}/2$ SIGNAL AND IS ALSO USED TO CONTROL MULTIPLEXER OF VIDEO OUTPUT.
	2	$\overline{\text{DISP1}}$	INPUT	$\overline{\text{DISP1}}$ SIGNAL IS INPUTTED FROM ACRTC. $\overline{\text{DISP1}}$ INDICATES SCREEN DISPLAY PERIOD. ORDINARILY, SET "1" TO DISPLAY SIGNAL CONTROL (DSC) BIT OF ACRTC.
	1	$\overline{\text{CUD1}}$	INPUT	$\overline{\text{CUD1}}$ SIGNAL IS INPUTTED FROM ACRTC. $\overline{\text{CUD1}}$ IS LOADED WITH "LOW" LEVEL DURING GRAPHIC CURSOR DISPLAY PERIOD.
	6-10 16 19-28	MADO -MAD15	INPUT/ OUTPUT	MADO-MAD15 OF ACRTC ARE INPUTTED. THESE SIGNALS ARE USED AS FRAME BUFFER ACCESS ADDRESS IN ADDRESS CYCLE FOR MCYC = "LOW", AS DATA INPUT/OUTPUT FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER IN DATA TRANSFER CYCLE FOR MCYC = "HIGH".
	29-32	MA16- MA19	INPUT	FRAME BUFFER ACCESS ADDRESS MA16 - MA19 IS INPUTTED FROM ACRTC.

O.G. FIG.		SUBCLASS	
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FIG. 3b

ITEM	TERMI- NAL NO.	TERMI- NAL NAME	INPUT/ OUTPUT	FUNCTION
FRAME BUFFER INTERFACE SIGNAL	50	\overline{RAS}	OUTPUT	\overline{RAS} TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	49	\overline{CS}	OUTPUT	\overline{CS} TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	48	\overline{WE}	OUTPUT	\overline{WE} TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	53	\overline{OE}	OUTPUT	\overline{OE} TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	56,58 60,62 63,61 59,57 55,54	FA0 - FA 9	OUTPUT	MULTIPLEX ADDRESS IS OUTPUTTED FOR DRAM. ADDRESS TO BE MULTIPLEXED VARIES DEPENDING ON VCF 0-VCF 3 AND VMD 0 ATTRIBUTE CODES.
	44,46 47,45 40,42 43,41	FDO - FD 7	INPUT/ OUTPUT	FD IS 8-BIT INPUT/OUTPUT SIGNAL FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER AND FOR FETCHING DISPLAY DATA READ FROM FRAME BUFFER. IN A CASE OF ONE MEMORY CHIP, FD 0-FD 3 ARE USED, WHEREAS IN A CASE OF TWO FOUR MEMORY CHIPS, FD 0-FD 7 ARE USED.
CRT DISPLAY INTERFACE SIGNAL	3	DOTCLK	OUTPUT	DOTCLK SIGNAL IS DELIVERED BY DIVIDING INCLK SIGNAL AS BASIC INPUT SIGNAL OF MIVAC BY 1, 2 AND 4. DIVISION RATIO IS SET DEPENDING ON VCF 0-VCF 3 OF ATTRIBUTE CODE.
	33, 34 36, 37	VIDEO A -VIDEO D	OUTPUT	VIDEO A-D SIGNAL IS 4-BIT OUTPUT SIGNAL WHICH IS OBTAINED BY CONVERTING DISPLAY DATA FROM PARALLEL SIGNAL INTO SERIAL SIGNAL BY SHIFT REGISTER OF MIVAC AND WHICH IS DELIVERED DURING DISPLAY PERIOD INDICATED BY SHIFTEN OUTPUT. 4-BIT VIDEO SIGNAL IS DETERMINED BY ATTRIBUTE CODE VCF 0-VCF 3.
	5	SHIFTEN	OUTPUT	SHIFEN INDICATES DISPLAY PERIOD OF VIDEO SIGNAL AND IS SET TO "HIGH" LEVEL DURING DISPLAY PERIOD. IN SINGLE ACCESS, $\overline{DISP1}$ FROM ACRTC IS ELONGATED BACKWARD BY ONE CYCLE, AND IN DUAL ACCESS, $\overline{DISP1}$ IS ECONGATED BACKWARD BY TWO SYCLES SO AS TO PRODUCE THIS SIGNAL.
	4	VSYNC.2	OUTPUT	VSYNC/2 SIGNAL IS INPUTTED TO ACRTC. \overline{VSYNC} IS DIVIDED BY TWO FOR PRODUCING THIS SIGNAL.
OTHERS	38	$\overline{BL2IRQ}$	OUTPUT	$\overline{BL2IRQ}$ IS SET BY BLINK 2 (MA19) INPUTTED IN ATTRIBUTE CYCLE. DURING ATTRIBUTE CYCLE, WHEN BLINK 2 IS AT "HIGH" LEVEL, $\overline{BLINK2}$ IS SET TO "LOW" LEVEL.
	39	\overline{IRQCLR}	INPUT	\overline{IRQCLR} SIGNAL IS USED TO CLEAR $\overline{BL2IRQ}$ SIGNAL. WHEN "LOW" IS INPUTTED TO \overline{IRQCLR} , $\overline{BL2IRQ}$ IS CLEARED TO "HIGH" LEVEL.

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The diagram illustrates a video display control system with the following components and signal paths:

- Inputs (Left):** MAD 0-15, MA 16-19, AS, MCYC, DRAW, MRD, VSYNC, HSYNC, DISPT, CUDT, INCLK, 2CLK.
- Control and Timing Blocks:**
 - MA OUTPUT CONTROL (2000):** Receives MAD signals and outputs MA signals.
 - COLUMN ADDRESS COUNTER (2002):** Receives MA signals and outputs to MPX (2003).
 - MEMORY CONTROL (2005):** Receives MA signals and outputs to RAS, CS, OE, WE.
 - STATE DECODER (2007):** Receives INCLK and outputs to VCF DECODER (2012).
 - 2CLK GENERATOR (2008):** Receives INCLK and outputs to INCLK DIVIDER (2009).
 - INCLK DIVIDER (2009):** Outputs to MPX (2010) and DOTCLK.
 - ATTRIBUTE LATCH (2011):** Receives DISPT and outputs to VCF DECODER (2012).
 - VCF DECODER (2012):** Outputs to FD OUTPUT CONTROL (2013).
 - FD OUTPUT CONTROL (2013):** Outputs to MPX (2014) and FDO, FD7.
 - INPUT DATA (2015):** Receives MRD and outputs to READ DATA LATCH (2016) and MPX (2017).
 - READ DATA LATCH (2016):** Outputs to LATCH CONTROL (2018).
 - LATCH CONTROL (2018):** Outputs to DISPLAY DATA LATCH (2019).
 - DISPLAY DATA LATCH (2019):** Outputs to LATCH (2020).
 - LATCH (2020):** Outputs to MULTIPLEXER (2021).
 - SHIFTER CLOCK (2023):** Receives SHFTEN and outputs to MULTIPLEXER (2021).
 - MULTIPLEXER (2021):** Outputs to SHEW (2022) and CURSOR BLINK (2023).
 - SHEW (2022):** Outputs to MPX (2024).
 - CURSOR BLINK (2023):** Outputs to MPX (2024).
 - MPX (2024):** Outputs to MASK (2025).
 - MASK (2025):** Outputs to VIDEO A, VIDEO O.
- Other Components:**
 - MPX (2003):** Receives MA signals and outputs to FA0, FA9.
 - MPX (2010):** Receives INCLK and outputs to DOTCLK.
 - MPX (2014):** Receives FDO, FD7 and outputs to FDO, FD7.
 - MPX (2017):** Receives INPUT DATA and outputs to DISPLAY DATA LATCH (2019).
 - MPX (2024):** Receives SHEW and CURSOR BLINK signals and outputs to MASK (2025).
- Outputs (Right):** FA0, FA9, RAS, CS, OE, WE, DOTCLK, FDO, FD7, BL2IRQ, VSYNC/2, SHFTEN, VIDEO A, VIDEO O.

FIG. 5a

1-CHIP MEMORY

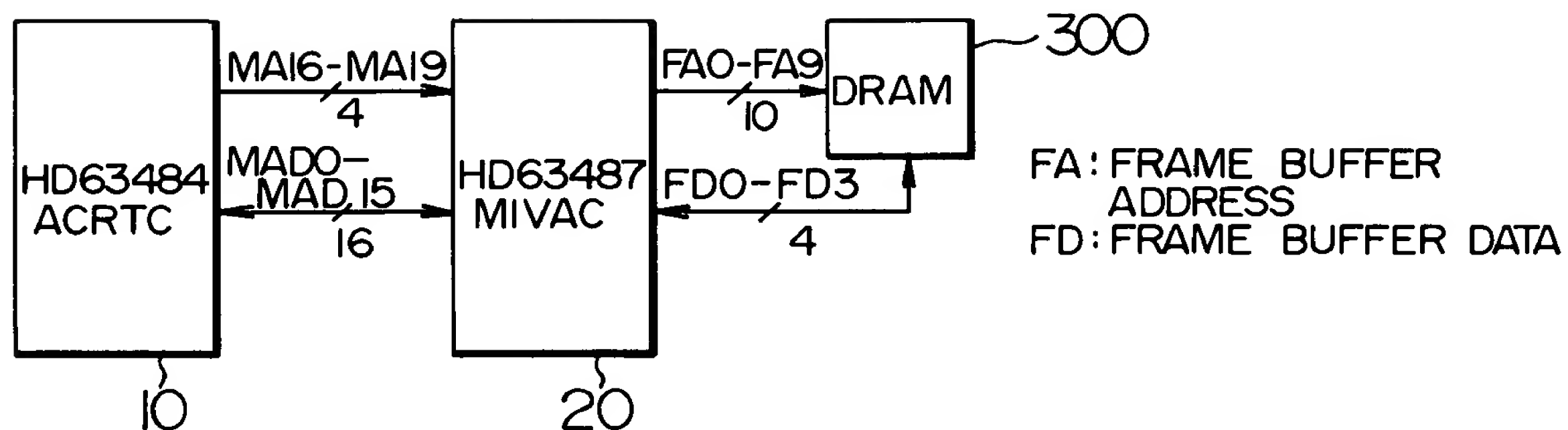


FIG. 5b

2-CHIP MEMORY

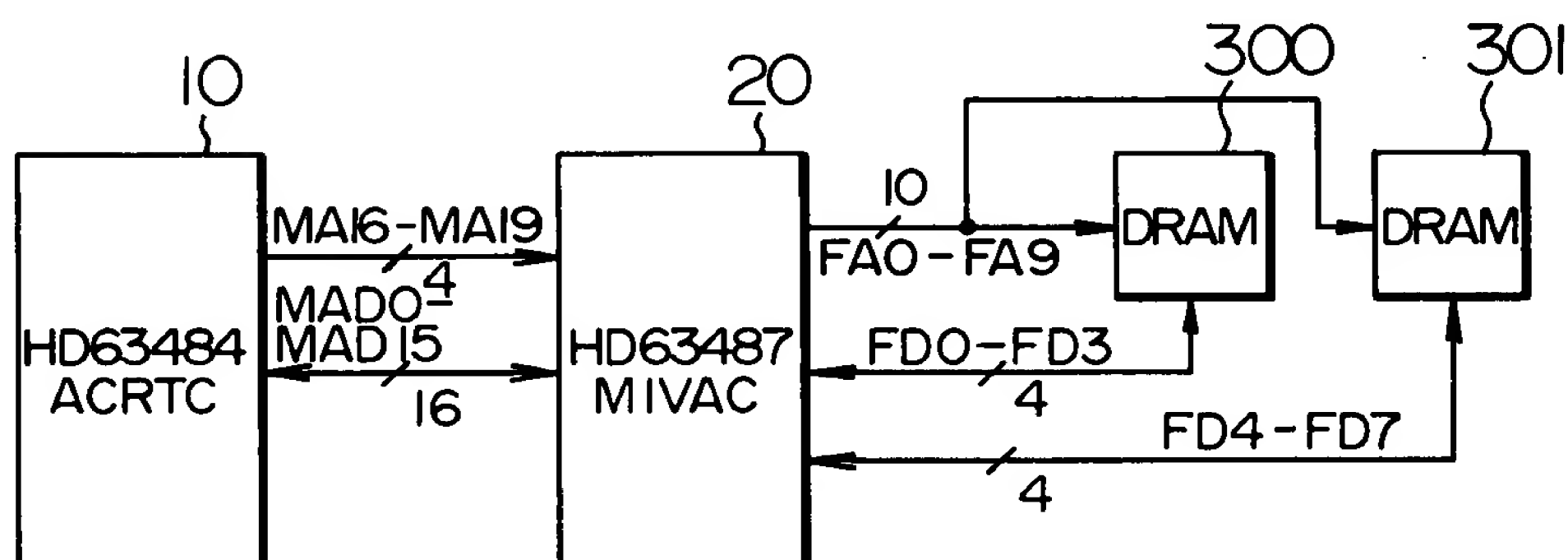
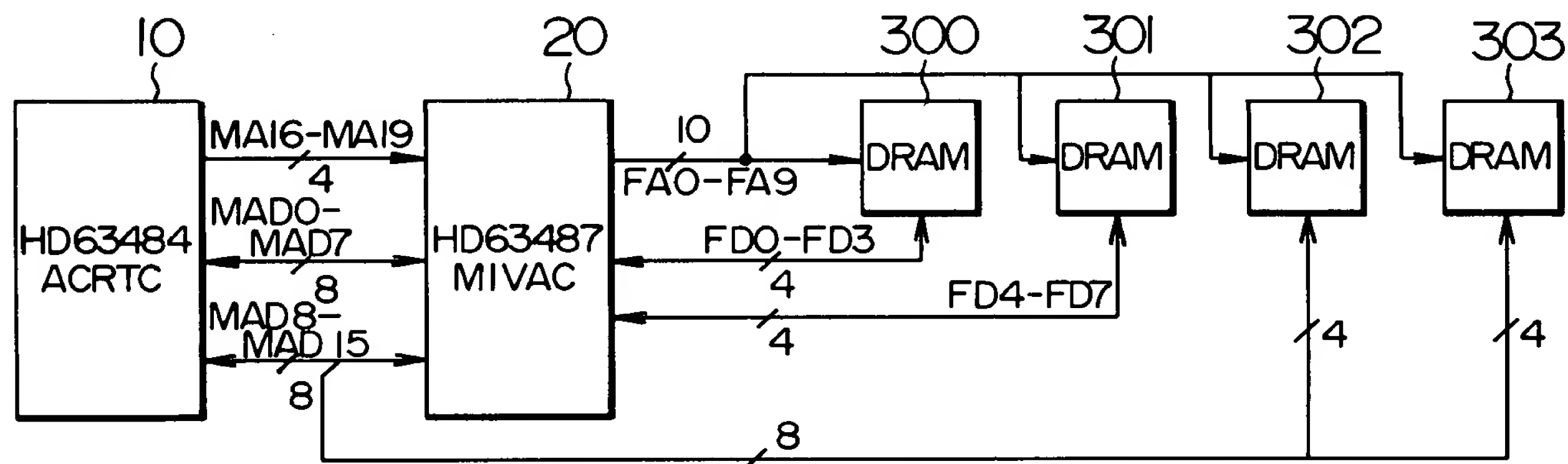


FIG. 5c

4-CHIP MEMORY



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FIG. 6

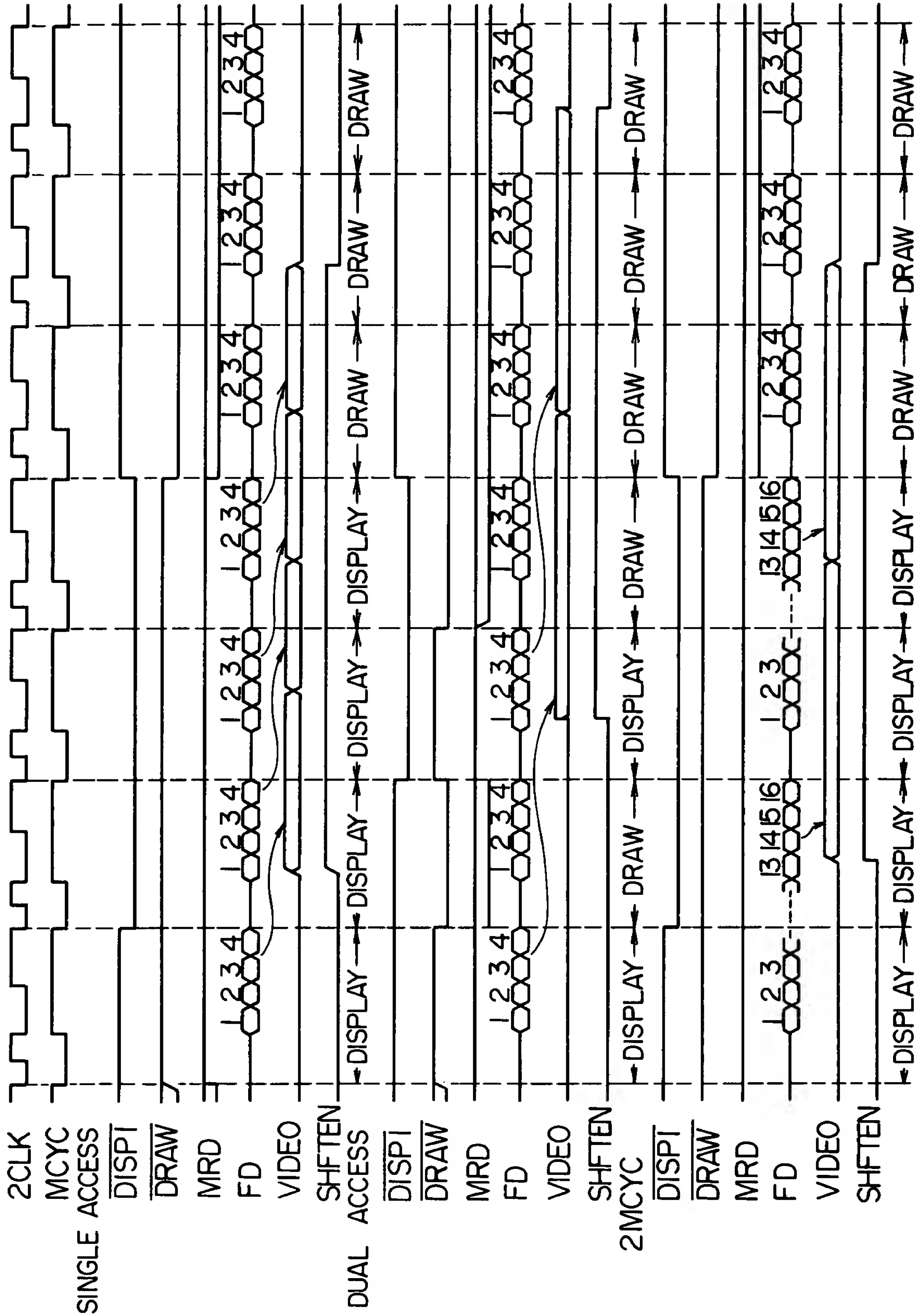


FIG. 7

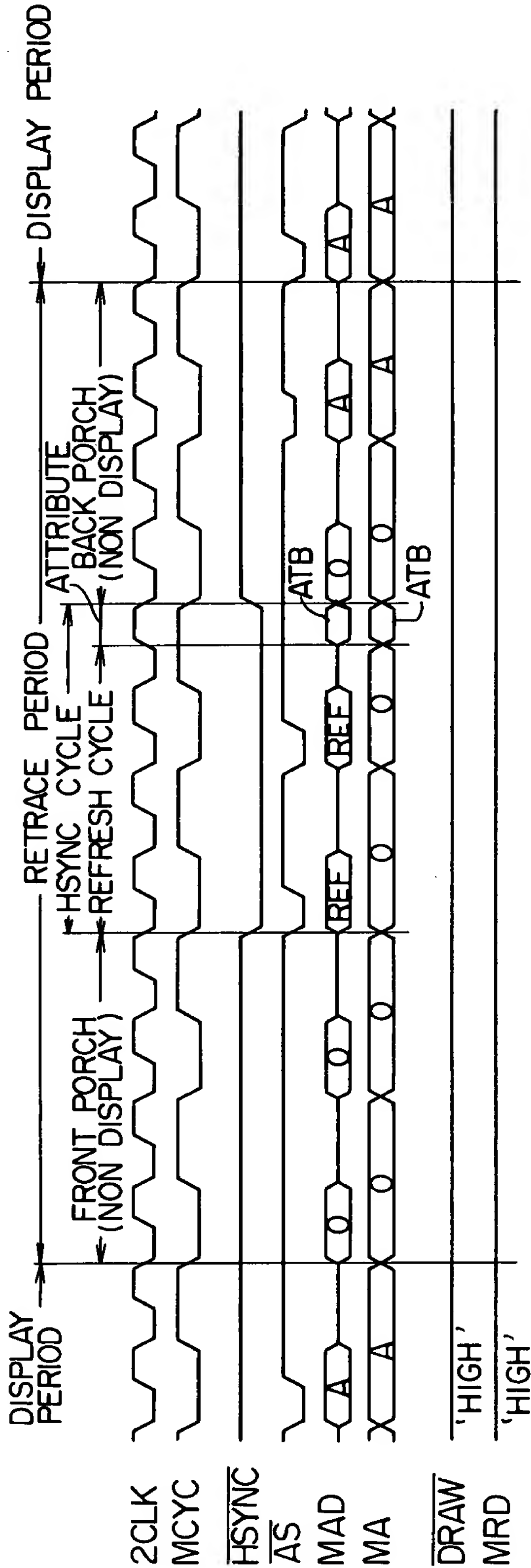
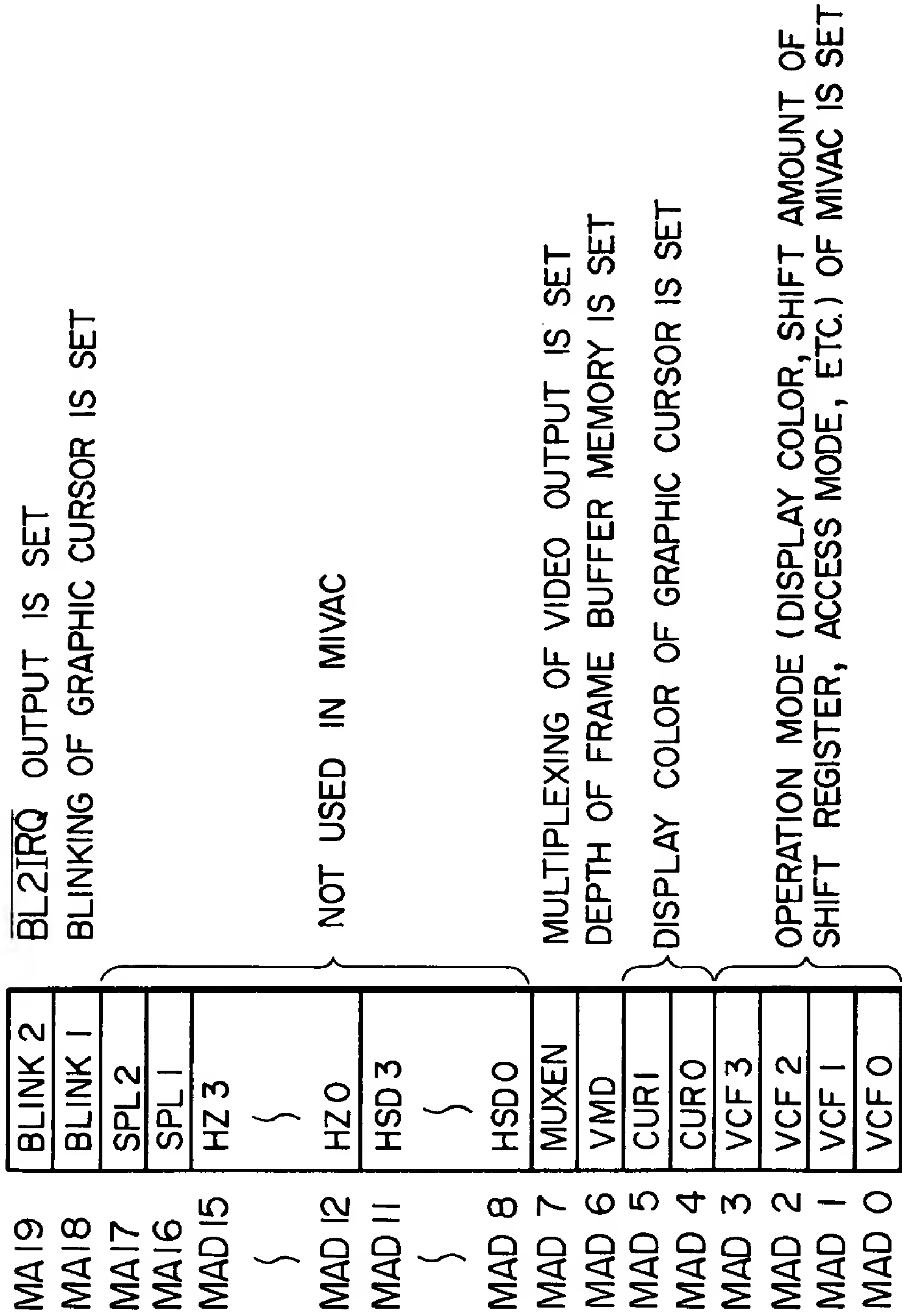


FIG. 11

CUR I	CUR O	CURSOR DISPLAY COLOR
0	0	BLACK (VIDEO A - VIDEO D = 0)
0	1	WHITE (VIDEO A - VIDEO D = 1)
1	0	COLOR REVERSION FOR EACH BIT OF VIDEO A - VIDEO D
1	1	COLOR REVERSION FOR EACH BIT OF VIDEO A - VIDEO D (VIDEO D IS KEPT UNCHANGED)

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FIG. 9

MODE	CRT SCREEN LAYOUT EXAMPLE (DOTS X RASTER)	MAXIMUM FRAME BUFFER CAPACITY (BYTES)	ACRTC OPERATION FREQUENCY (MHz)	MEMORY ACCESS SPEED	HIGH-SPEED DRAWING	NUMBER OF MEMORIES	COLOR/GRADATION	SHIFT AMOUNT (BITS)	MAXIMUM DOT CLOCK FREQ. (MHz)
0	640x200, 350, 400, 480		4.13	480 ns / 4 ACCESSSES	—	1	4	16	33
1	640x200, 480x240, 320x200, 240	512K / 128K							
2	320x200, 240, 266x192								
3	640x200, 350, 400, 480								
4	640x200, 480x240, 320x200, 240	1M / 256K							
5	640x200, 350, 400, 480	2M / 512K							
6	640x200, 480x240, 320x200, 240	512K / 128K							
7	320x200, 240, 256x192								
8	640x200, 350, 400, 480								
9	640x200, 480x240, 320x200, 240	1M / 256K							
A	320x200, 240, 256x192								
B	640x200, 350, 400, 480								
C	640x200, 480x240, 320x200, 240	2M / 512K							
D	640x200, 350, 400, 480								
E	640x200, 480x240, 320x200, 240	512K / 128K							
F	640x200, 350, 400, 480	1M / 256K							

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FIG. 10

MODE	DOT CLOCK FREQUENCY
0, 3, 5, 8 B, D, F	33MHz ~ 11MHz
1, 4, 6, 9 C, E	16.5MHz ~ 5.5MHz
2, 7, A	8.25MHz ~ 2.75MHz

FIG. 12

VMD	MEMORY CHIP EMPLOYED
0	256 K × 4BIT DRAM
1	1M × 4BIT DRAM

FIG. 13

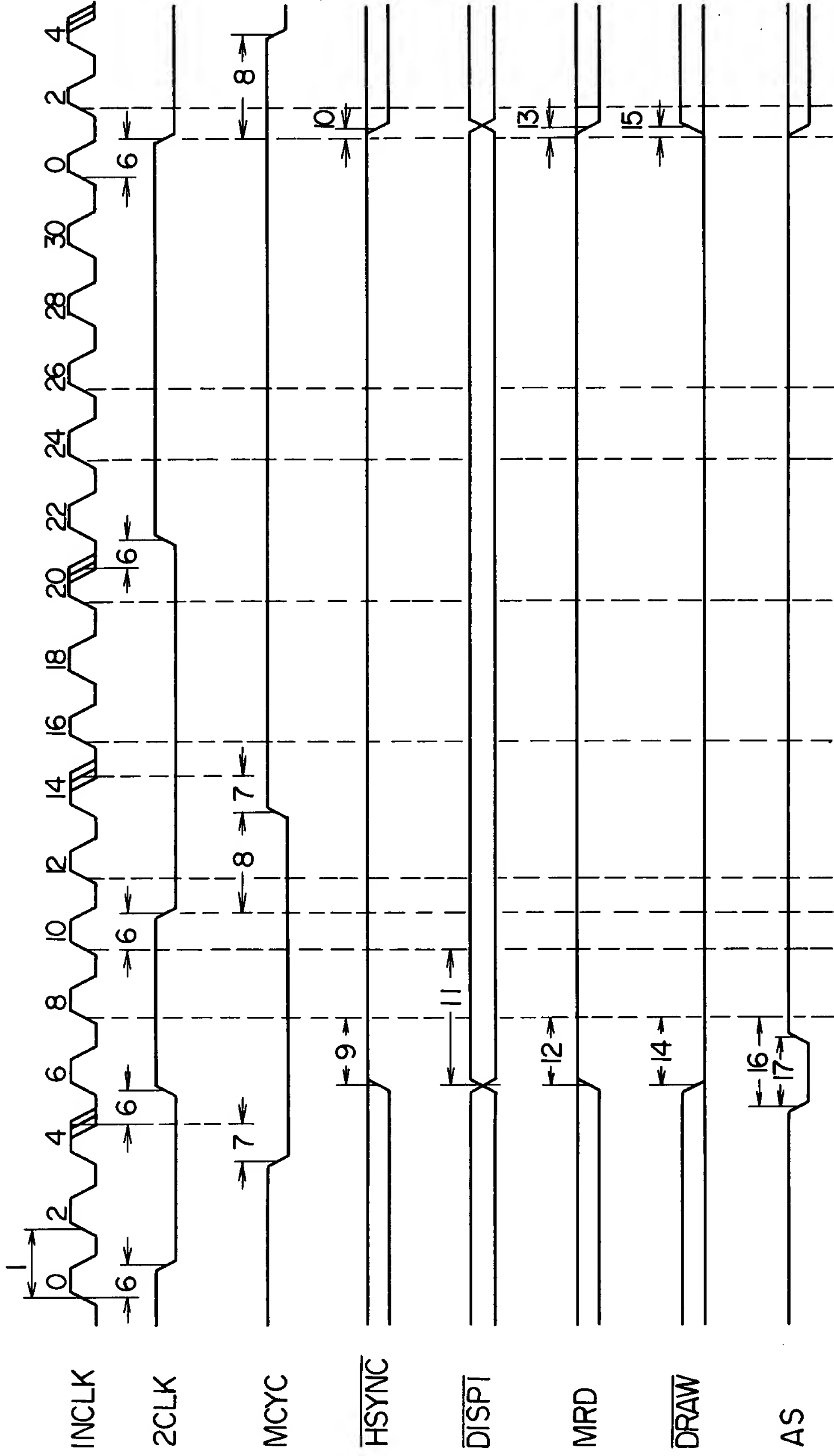
MUXEN	VSYNC / 2	VIDEO A	VIDEO B
0	0	A	B
	1	A	B
1	0	A	B
	1	C	D

FIG. 14

BLINK 1	GRAPHIC CURSOR DISPLAY
0	NOT DISPLAYED
1	DISPLAYED

O.G. FIG.	SUBCLASS	
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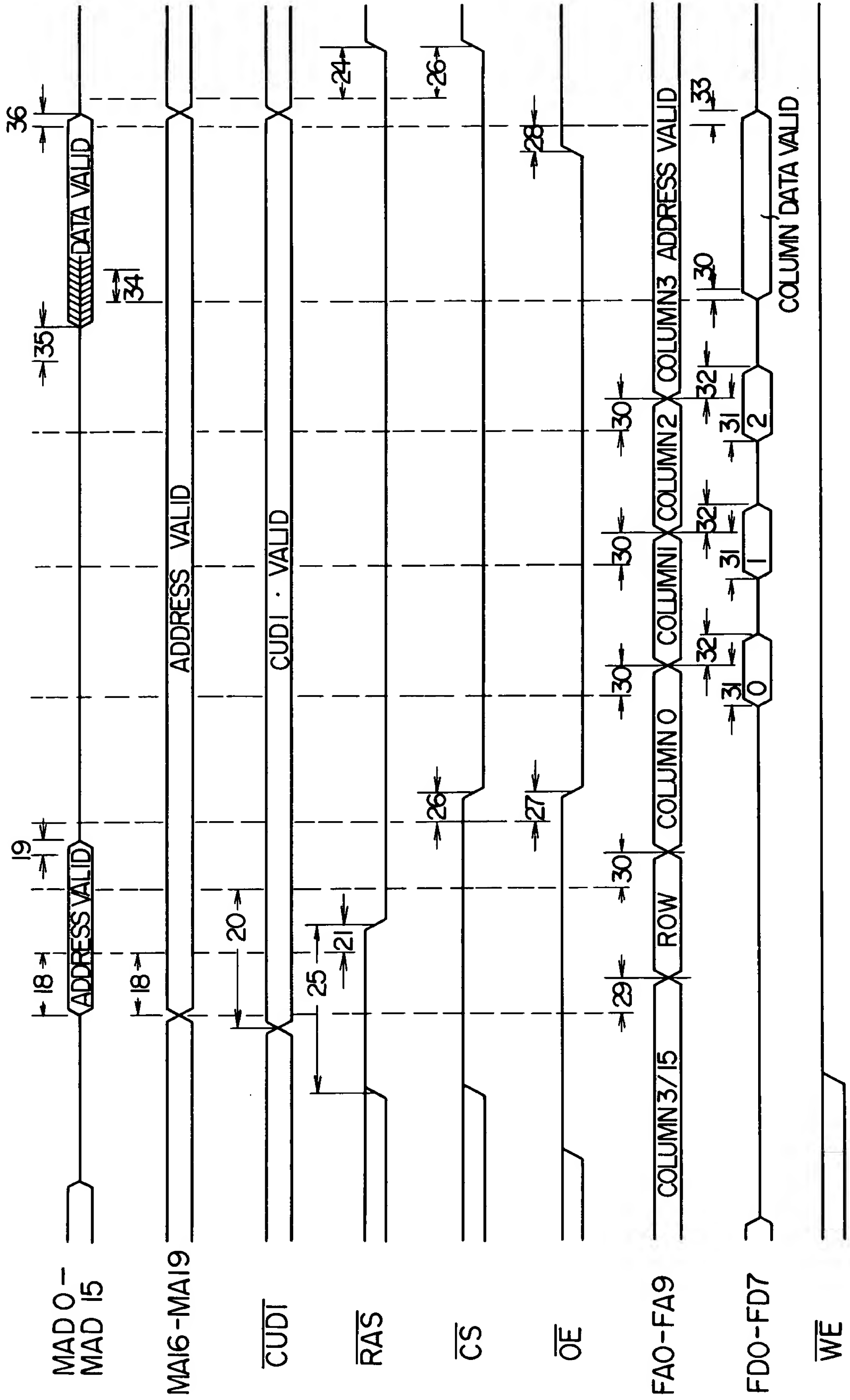
FIG. 15a



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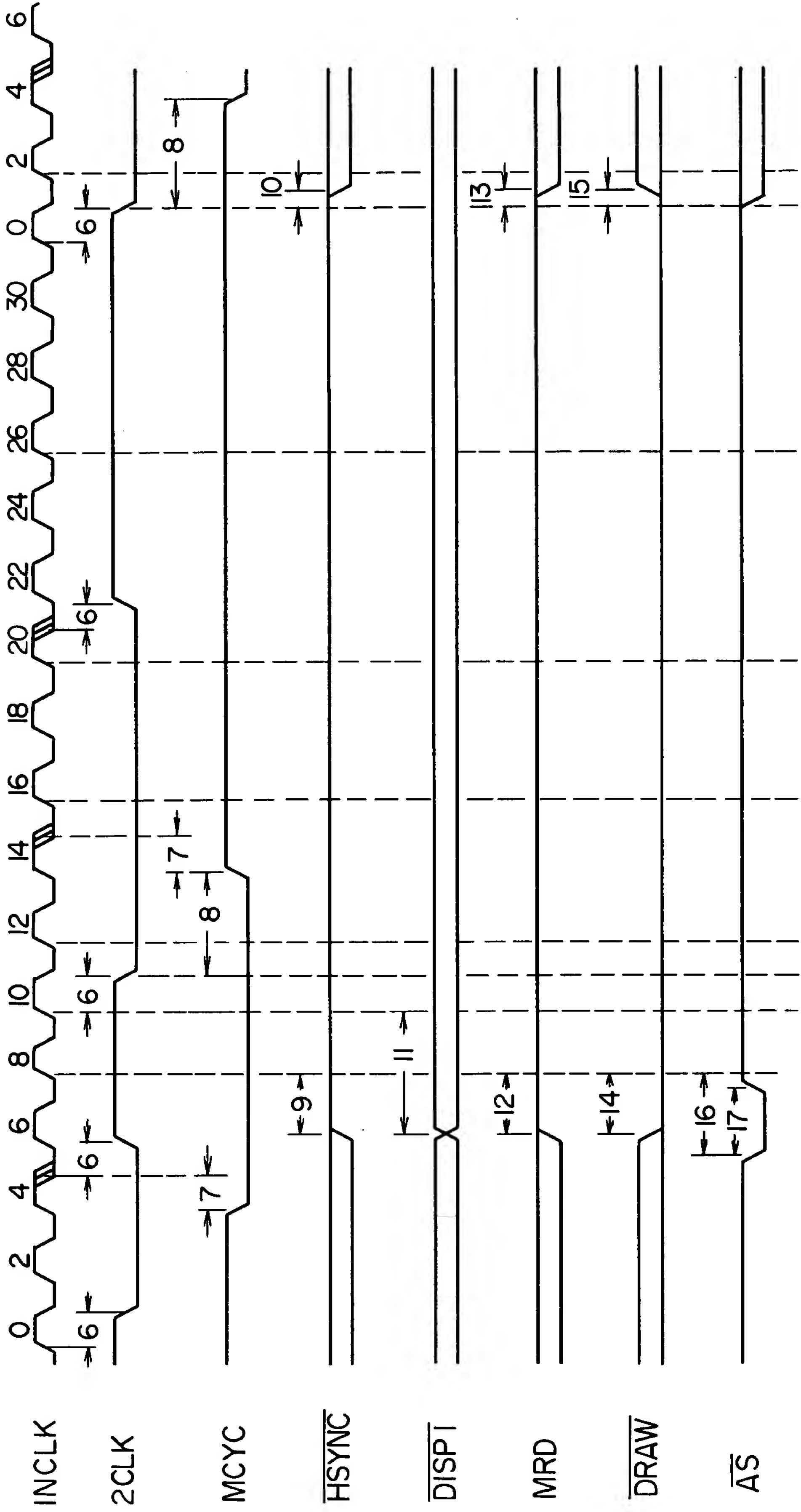
FIG. 15b

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APPROVED	O.G. FIG.	
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FIG. 16a



APPROVED	O.G. FIG.	
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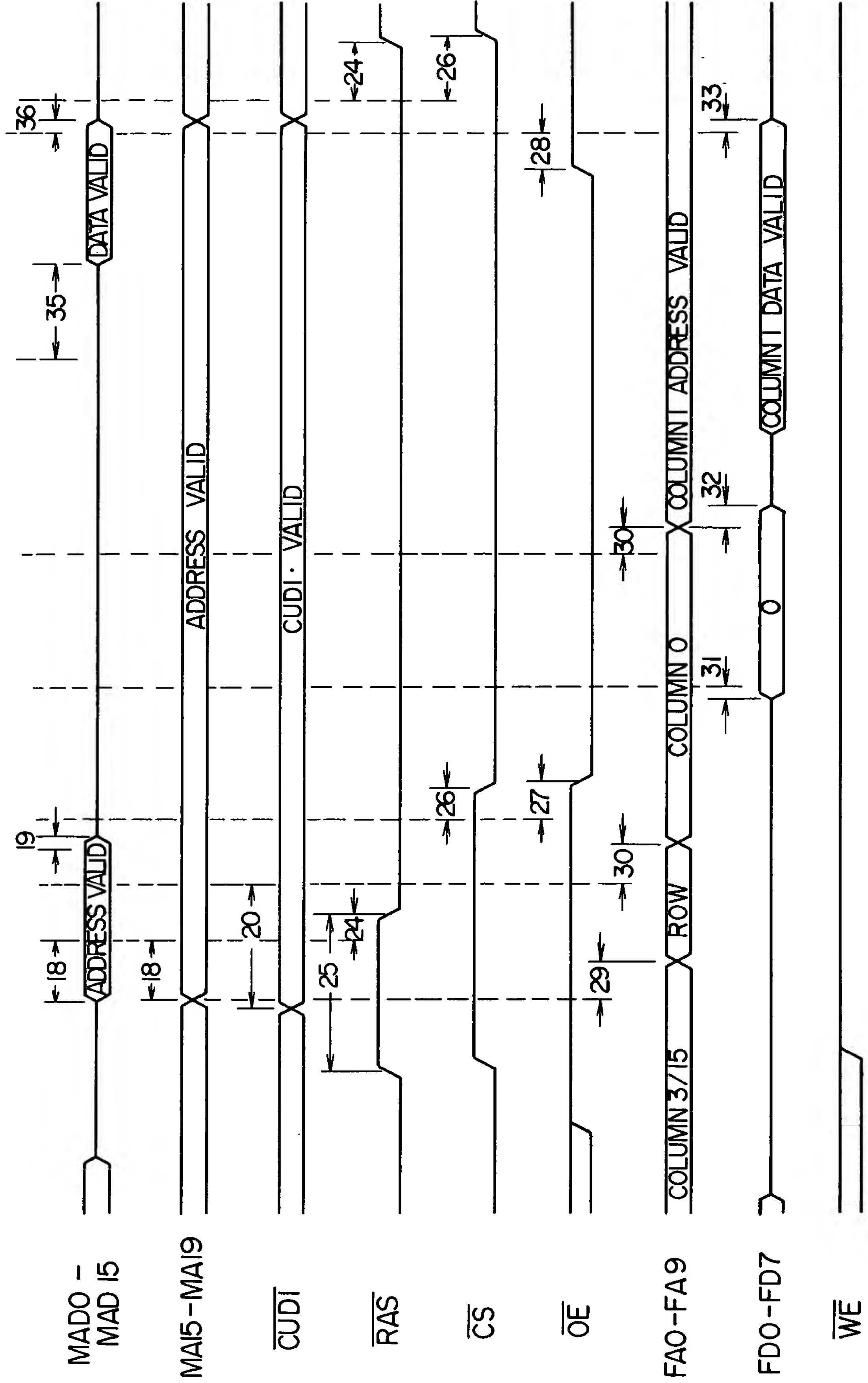
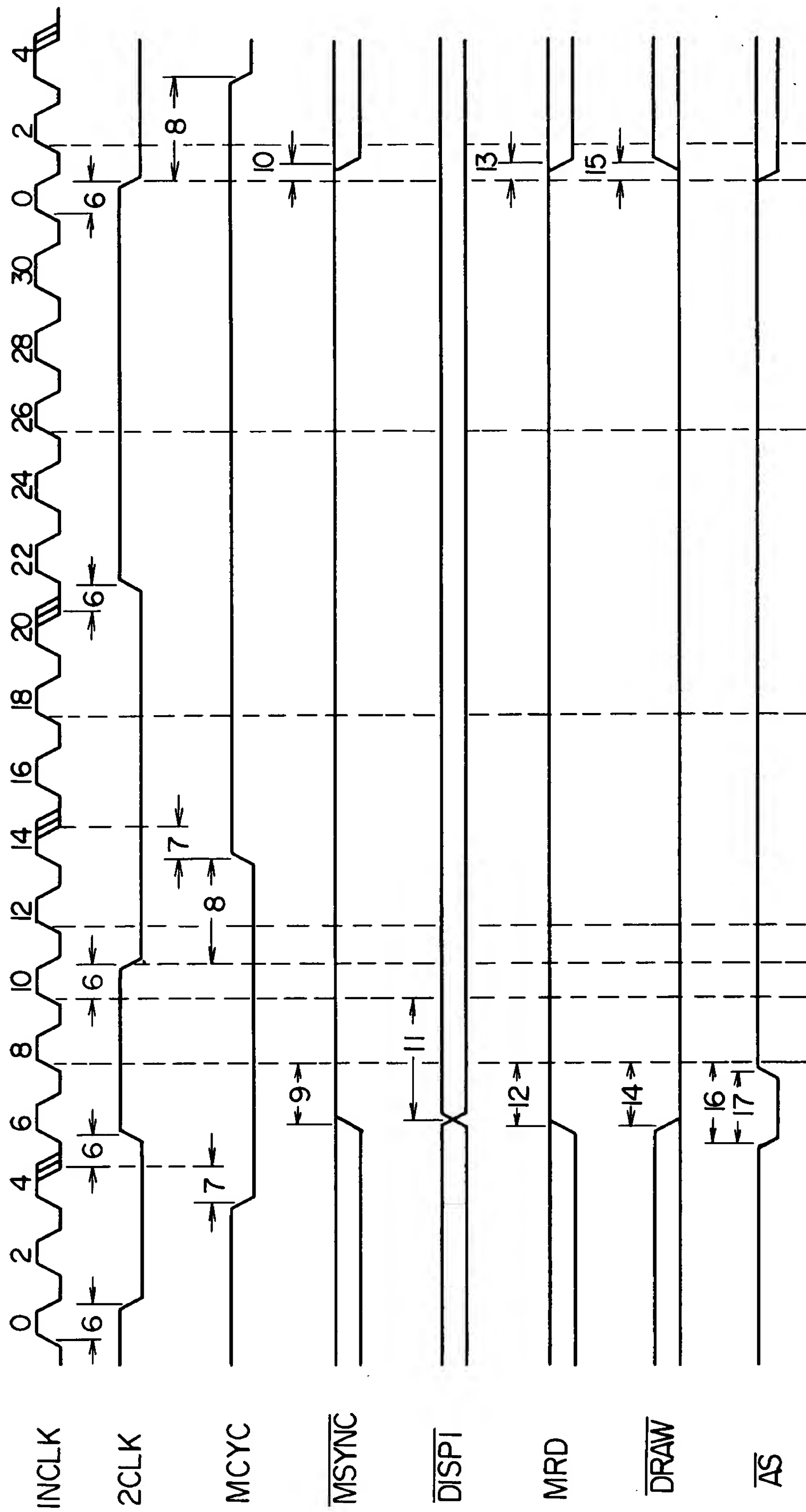


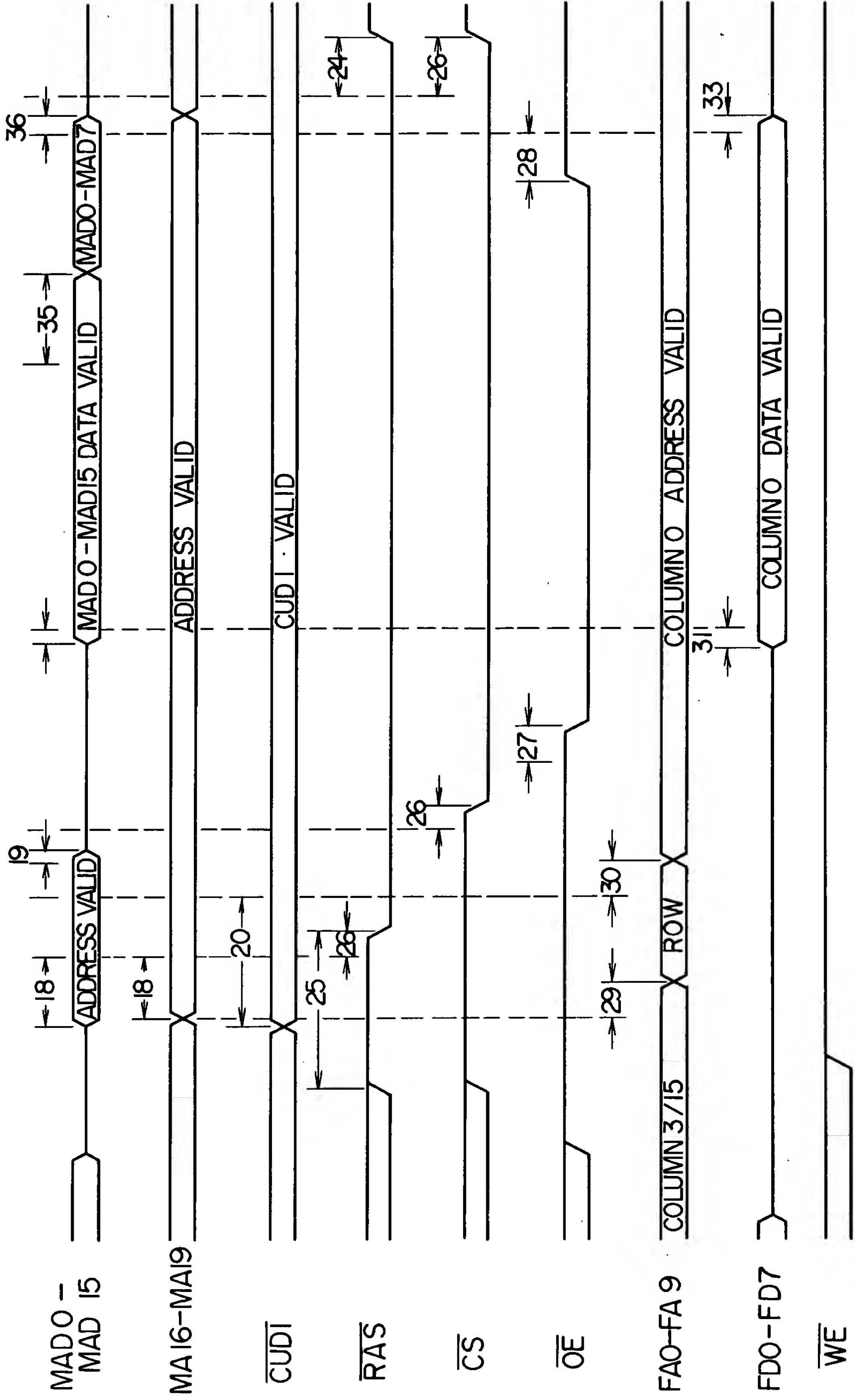
FIG. 17a



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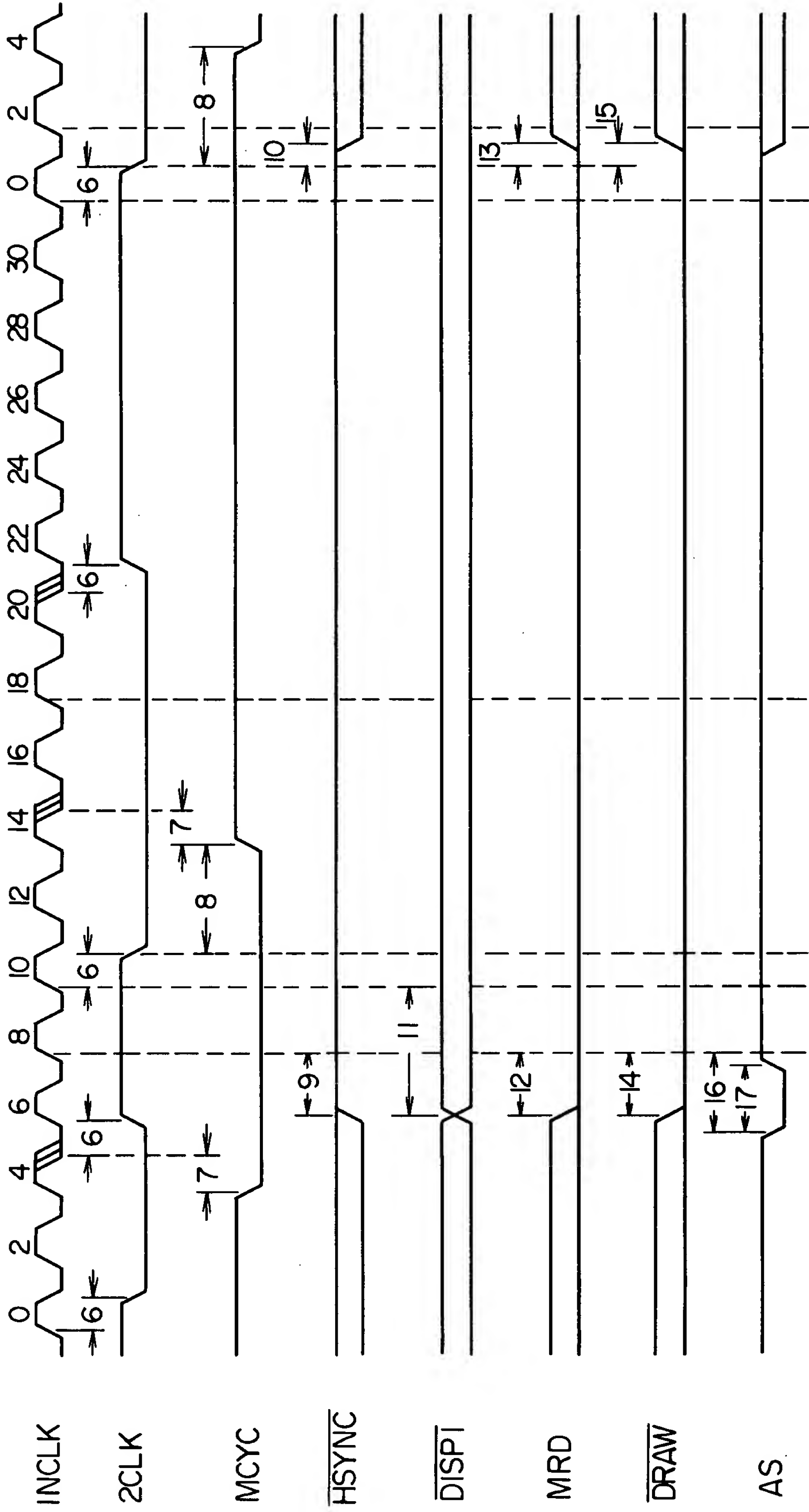
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FIG. 17b



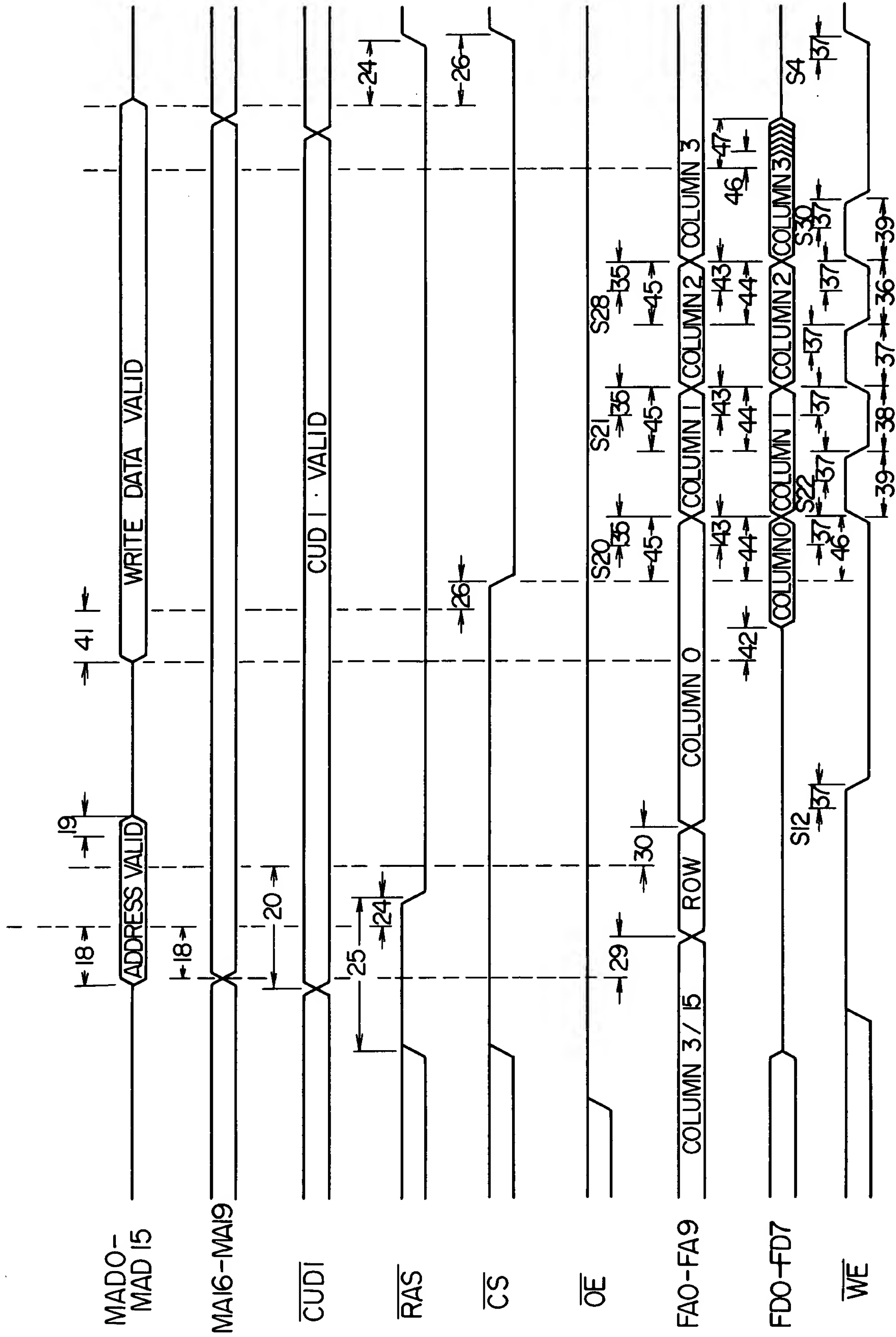
APPROVED	O.G. FIG.	
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FIG. 18a



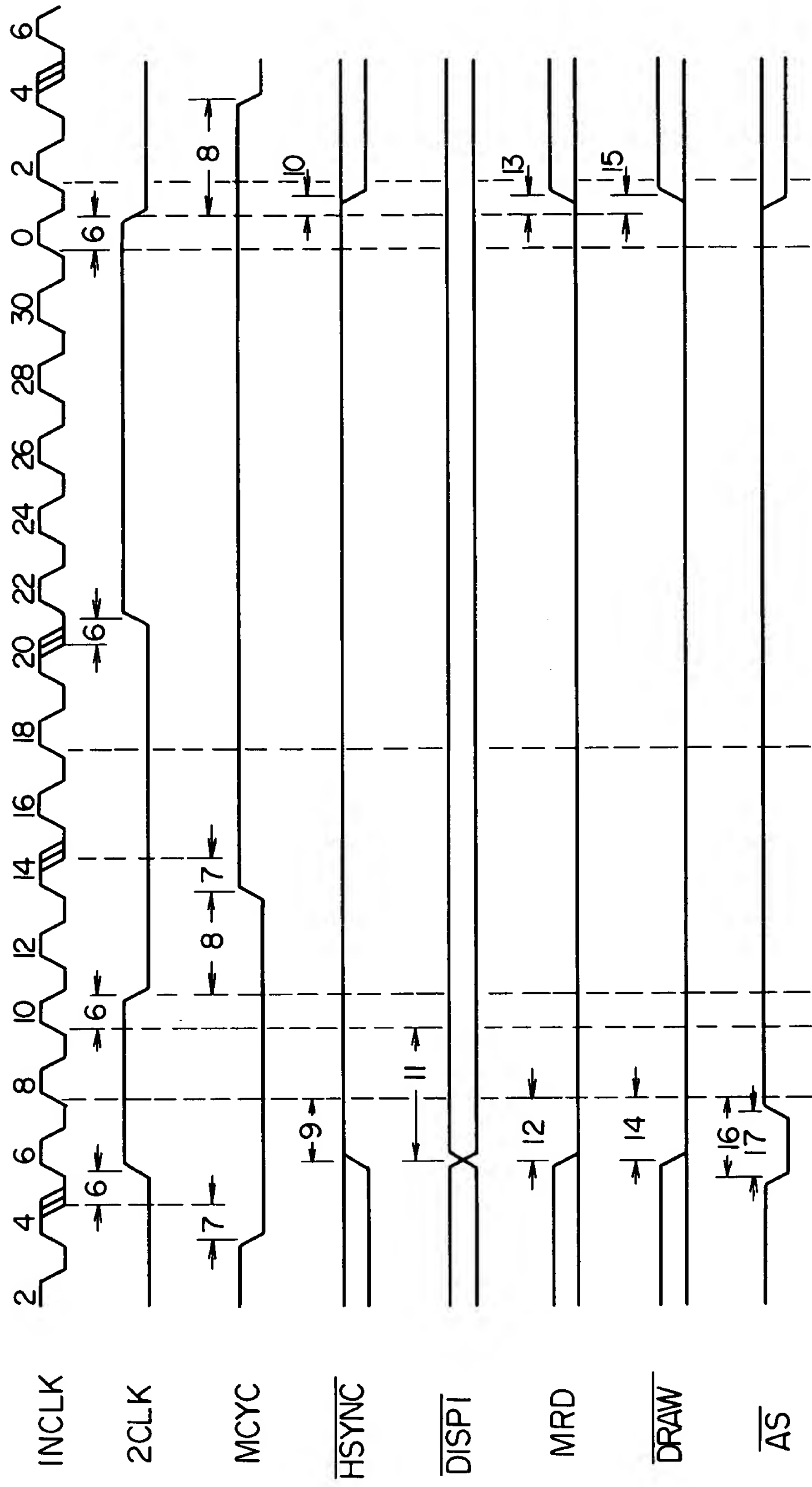
APPROVED	O.G. FIG.	
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FIG. 18b

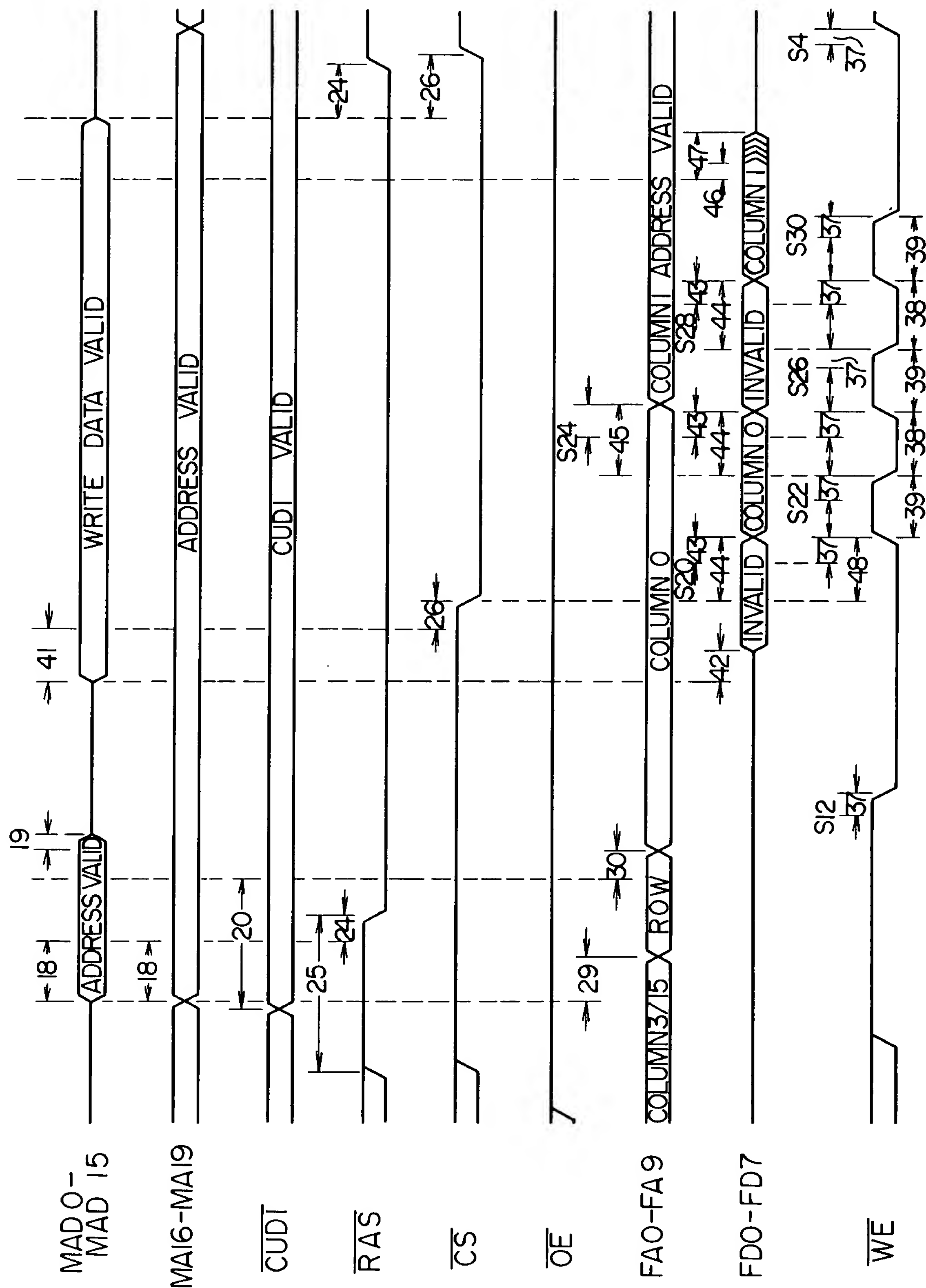


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FIG. 19a

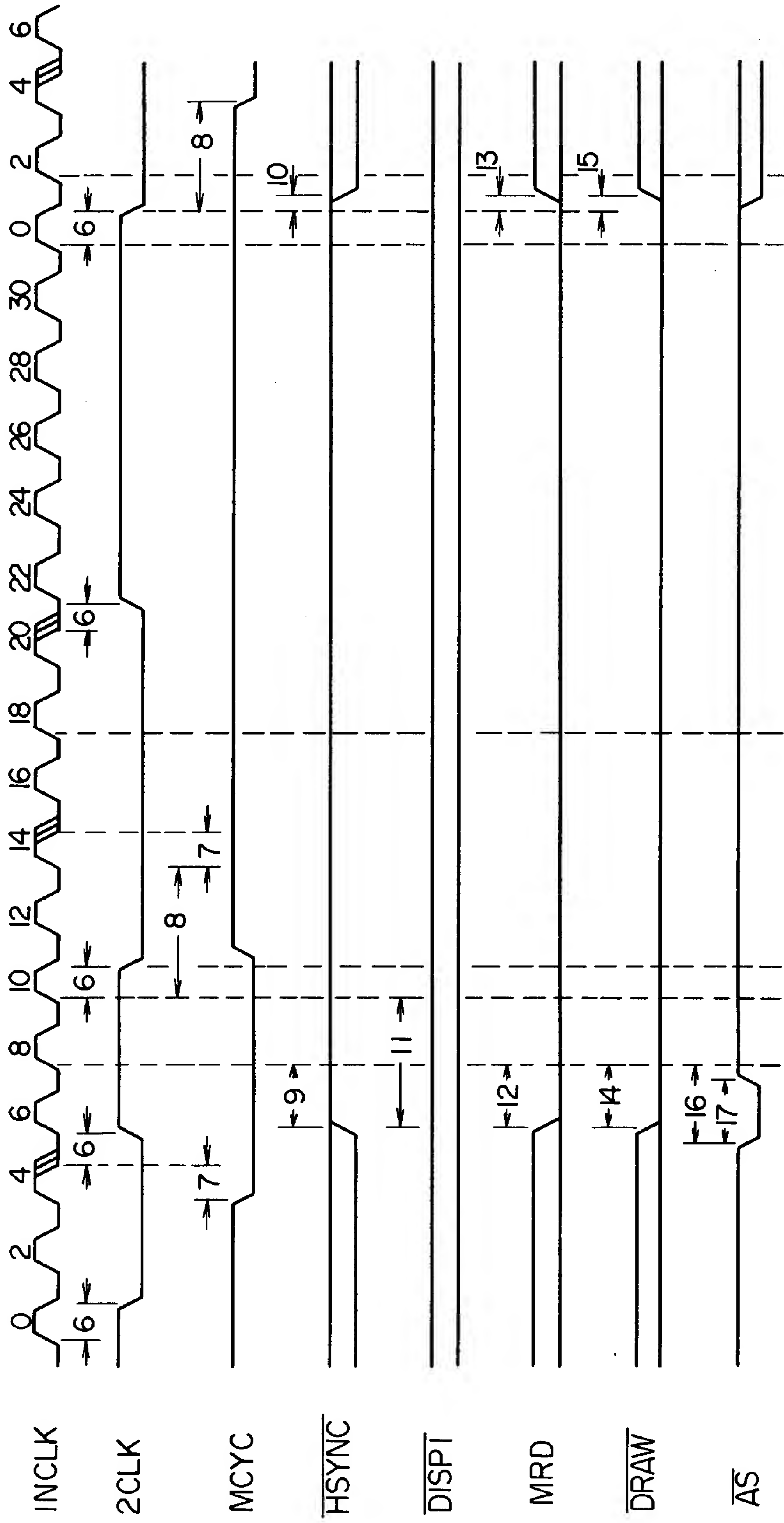


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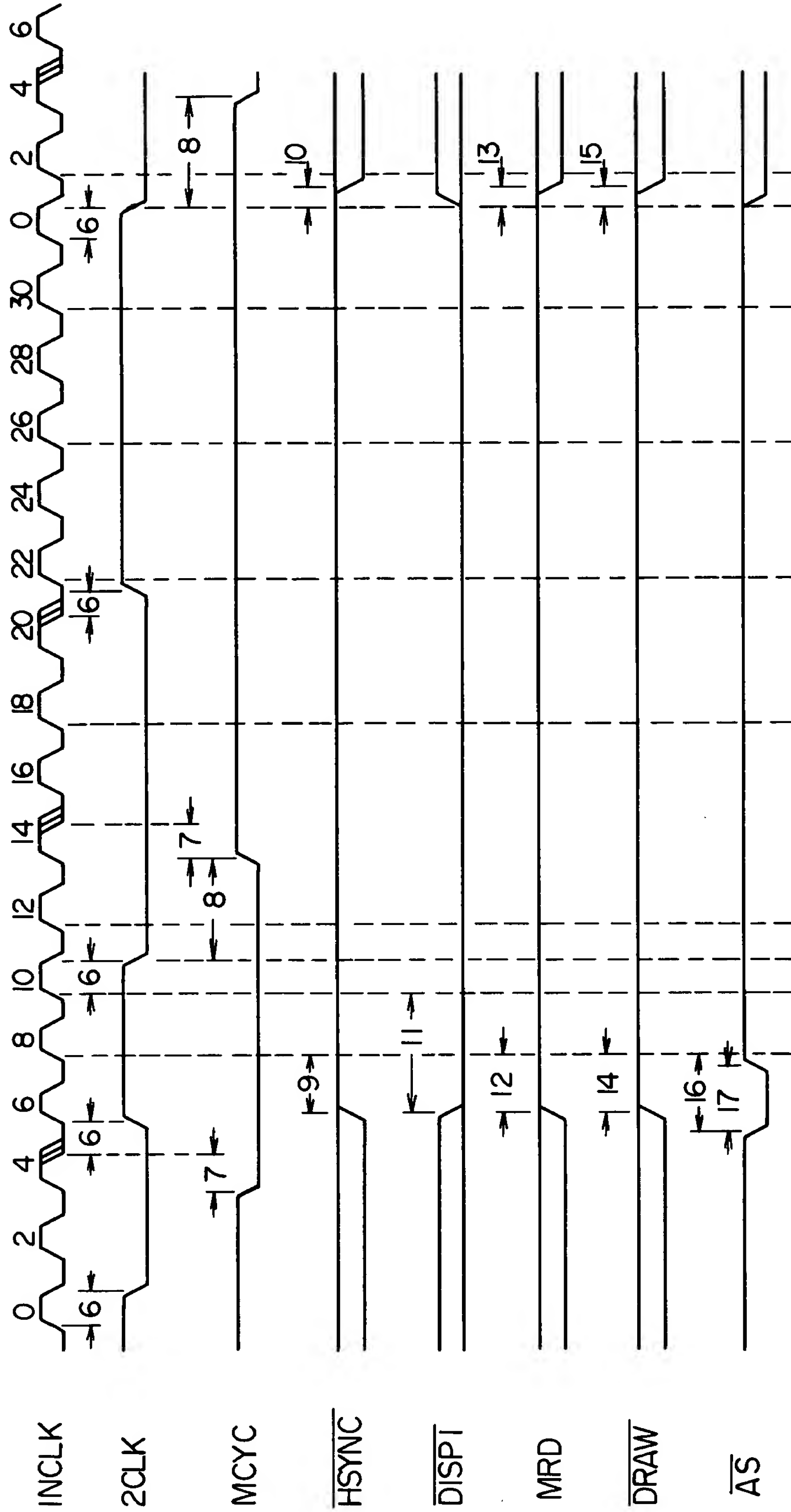
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FIG. 20a



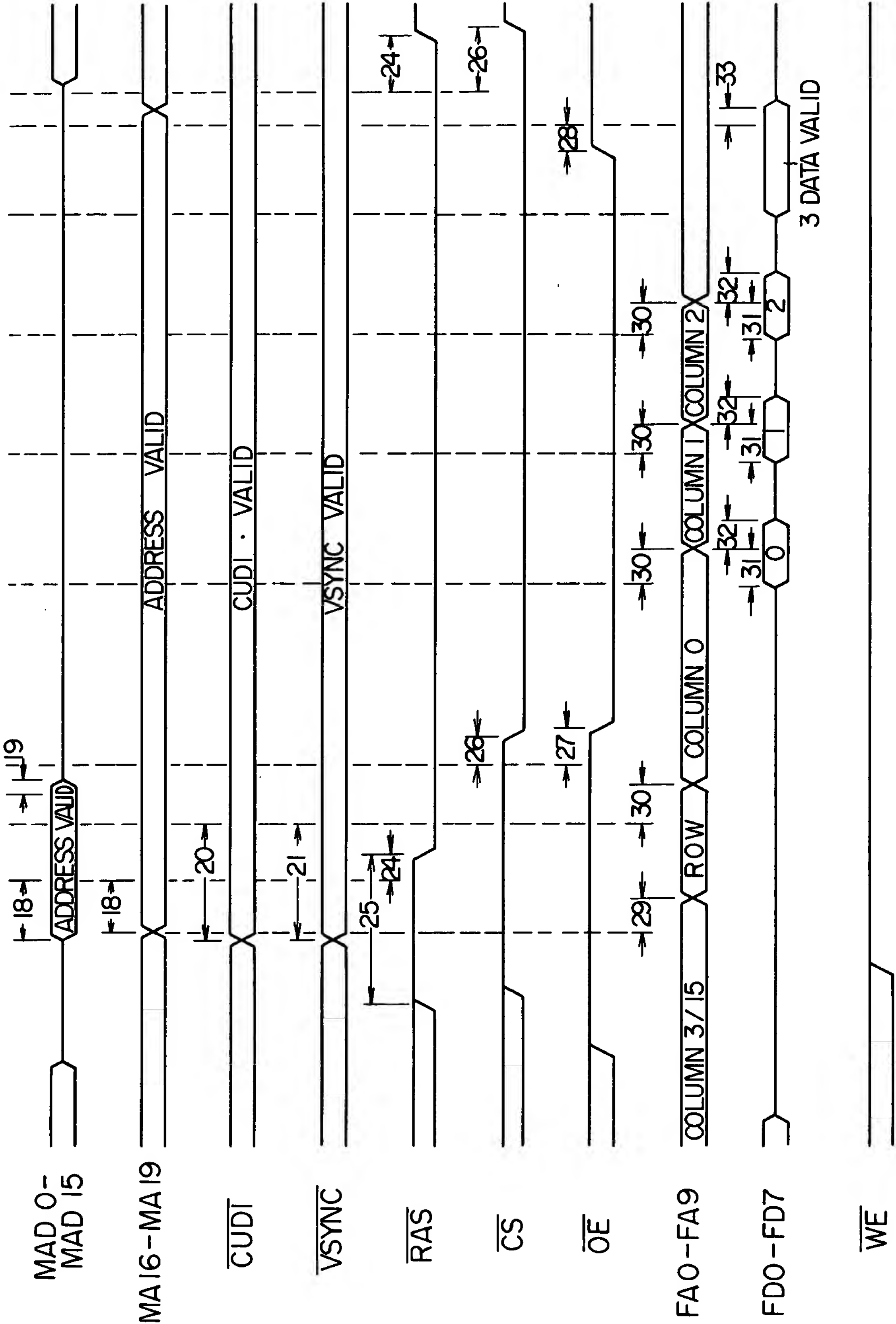
APPROVED	O.G. FIG.	
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FIG. 21a

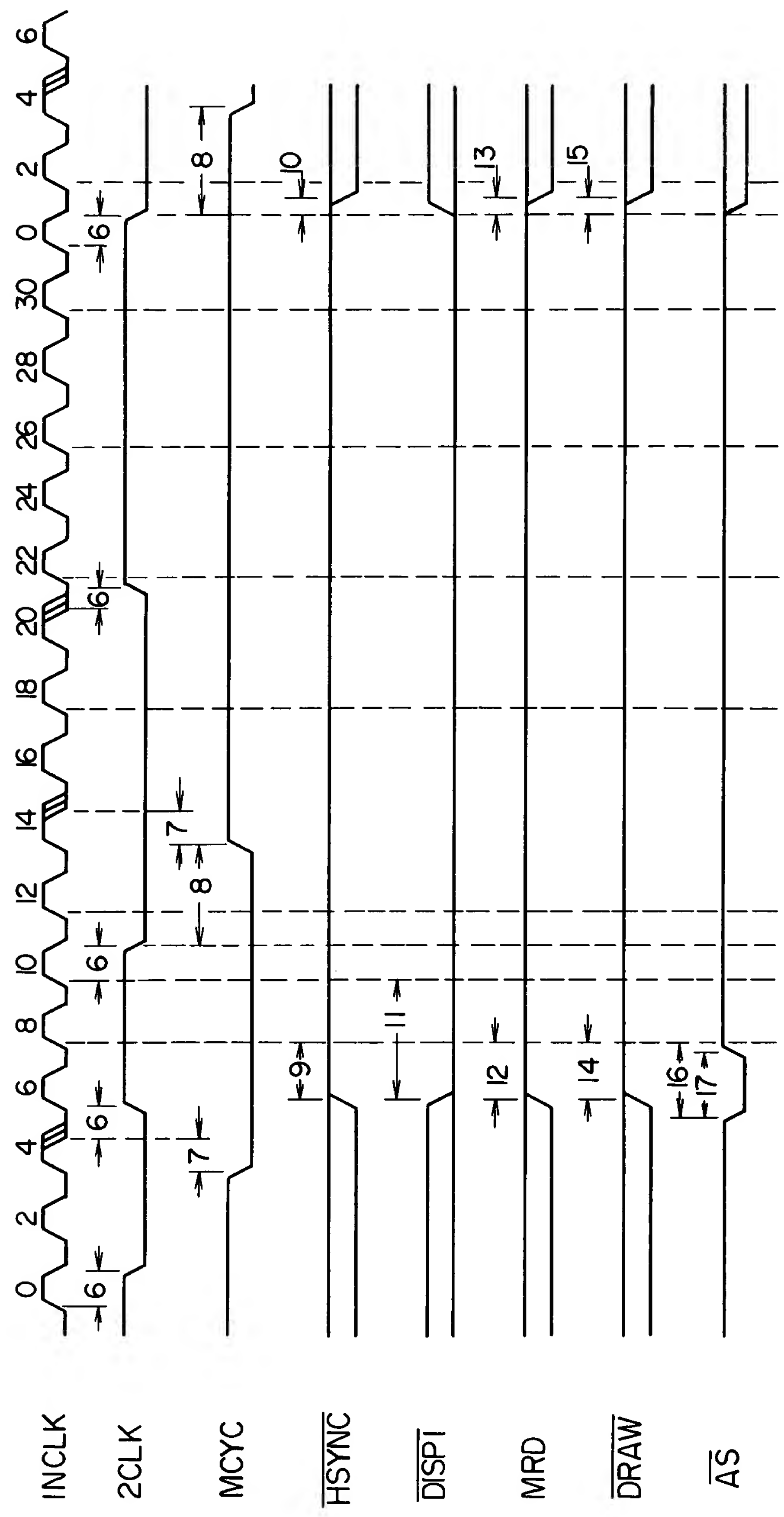


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F I G. 21b



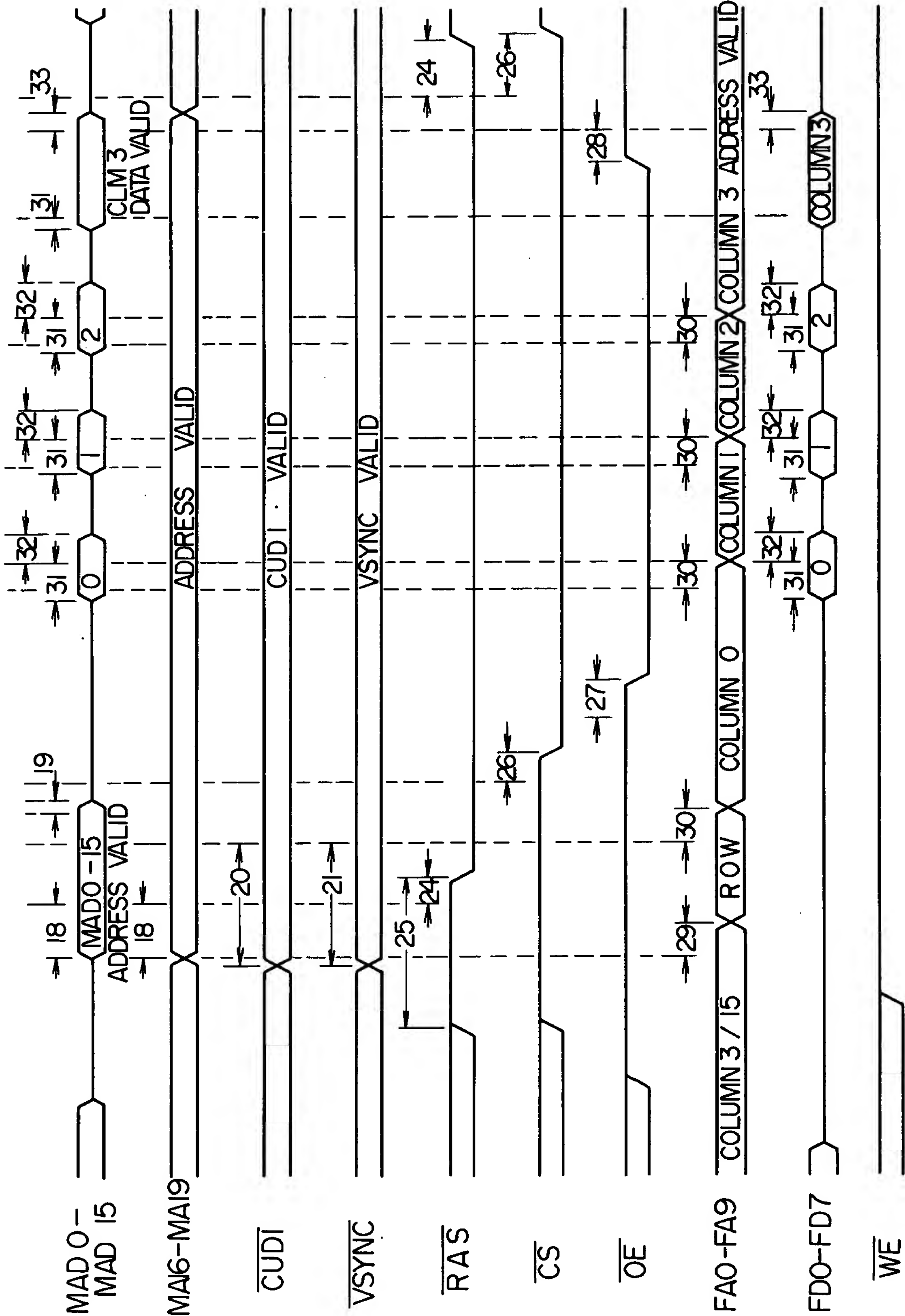
F I G. 22a



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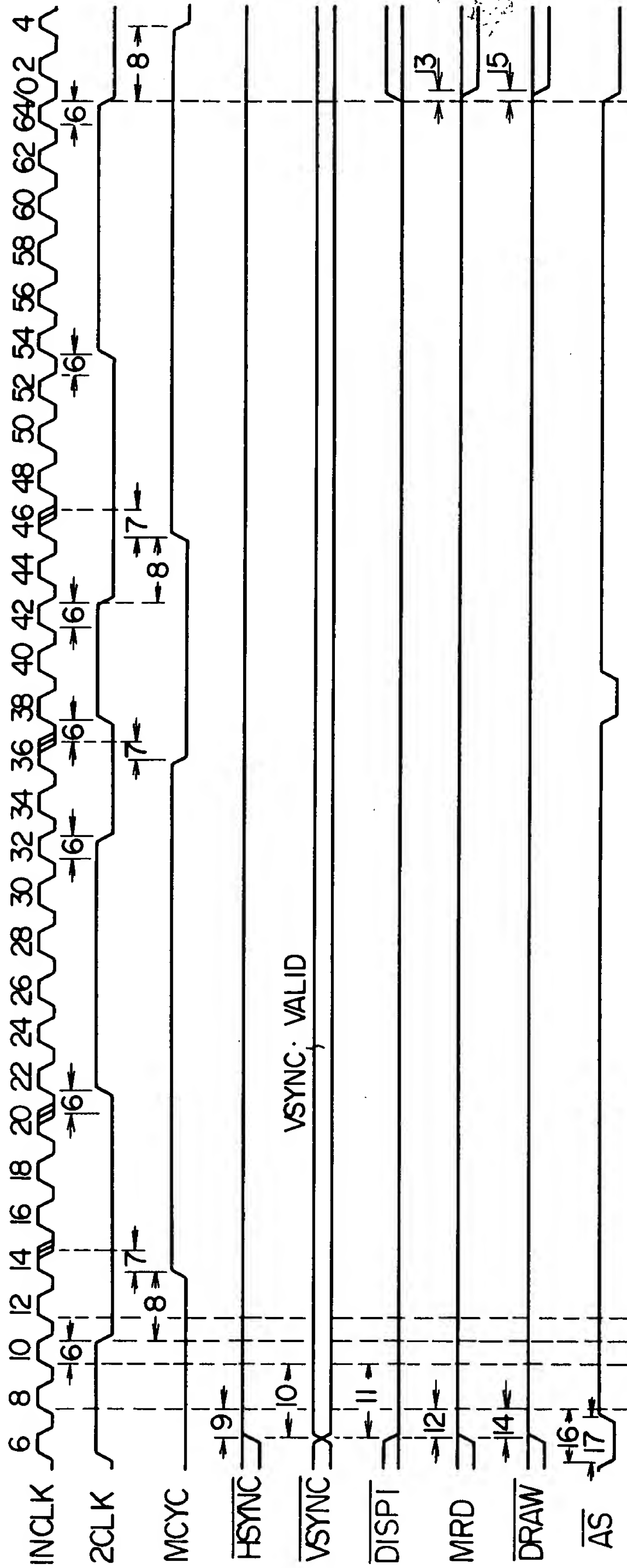
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F I G. 22b



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F I G. 23b

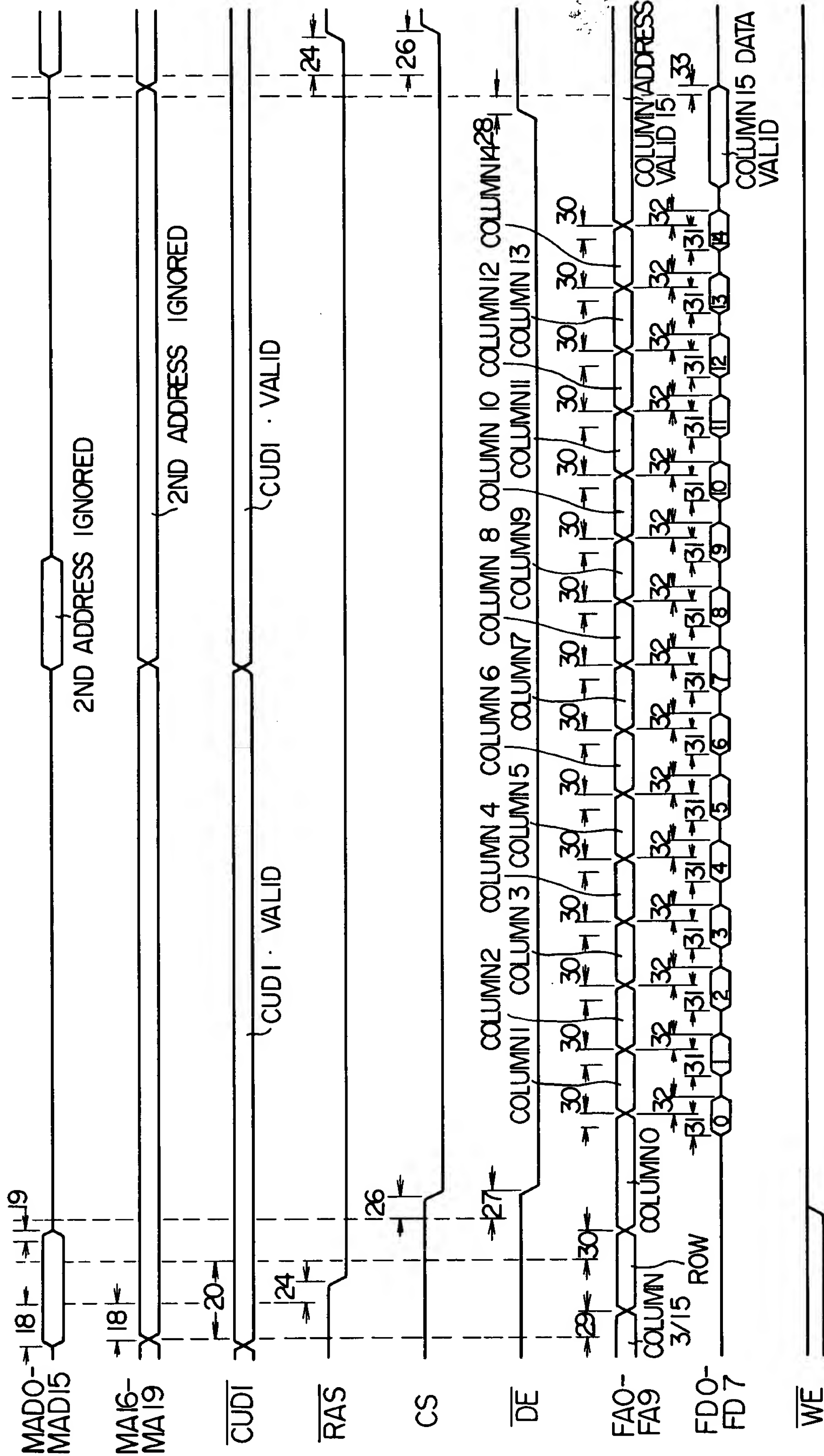
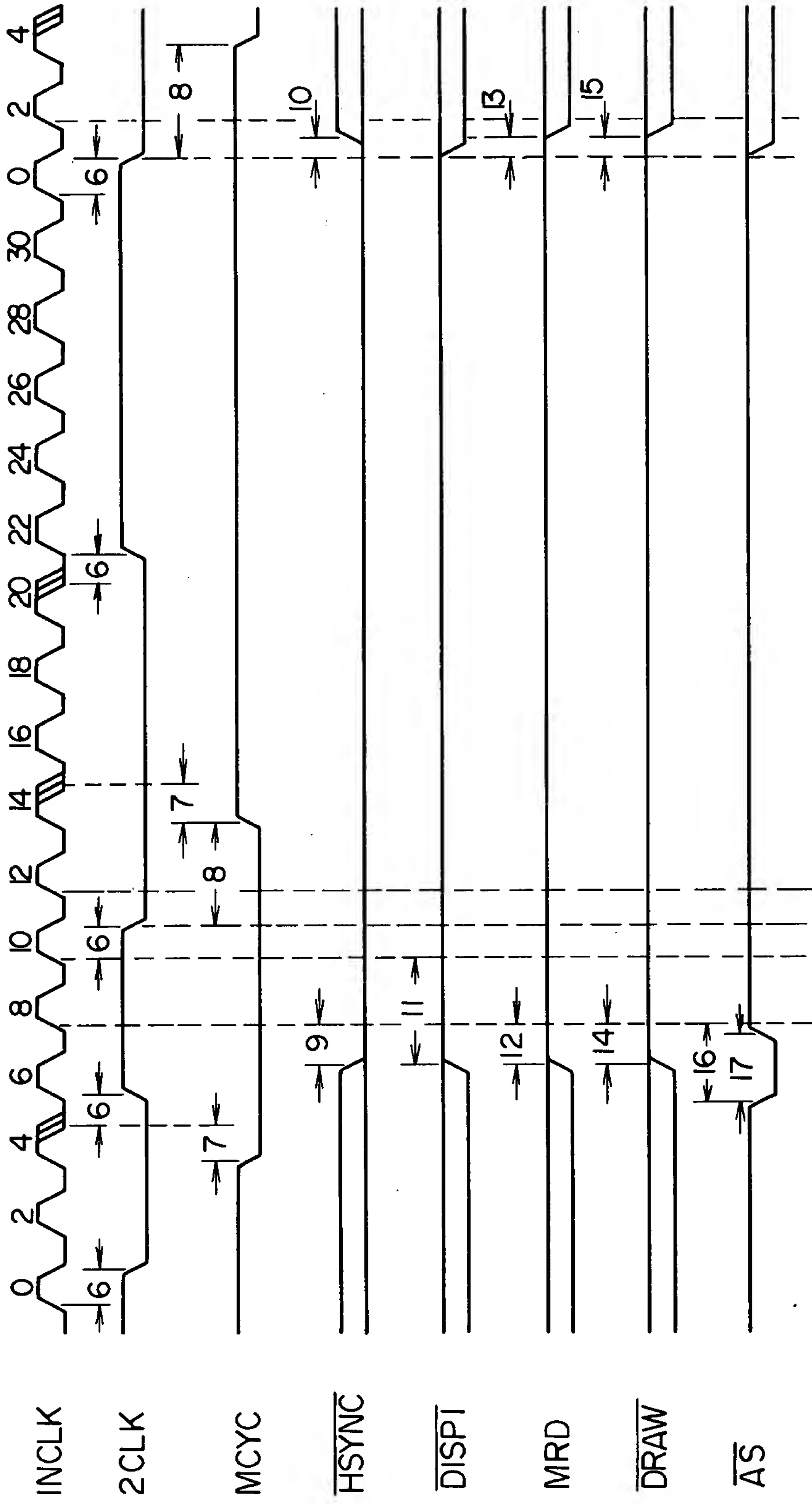


FIG. 24a



APPROVED	O.G. FIG.	
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FIG. 24b

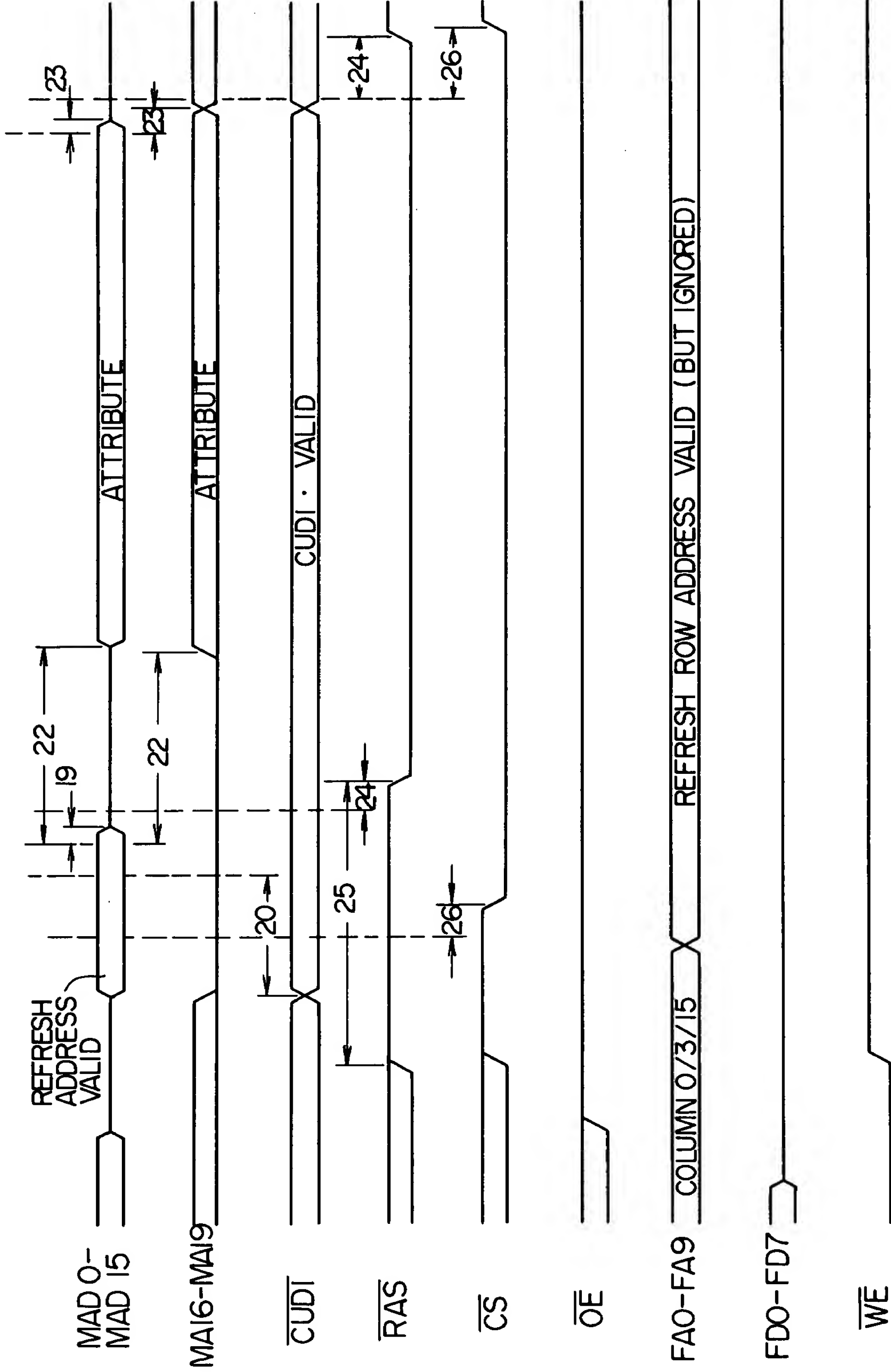


FIG. 25

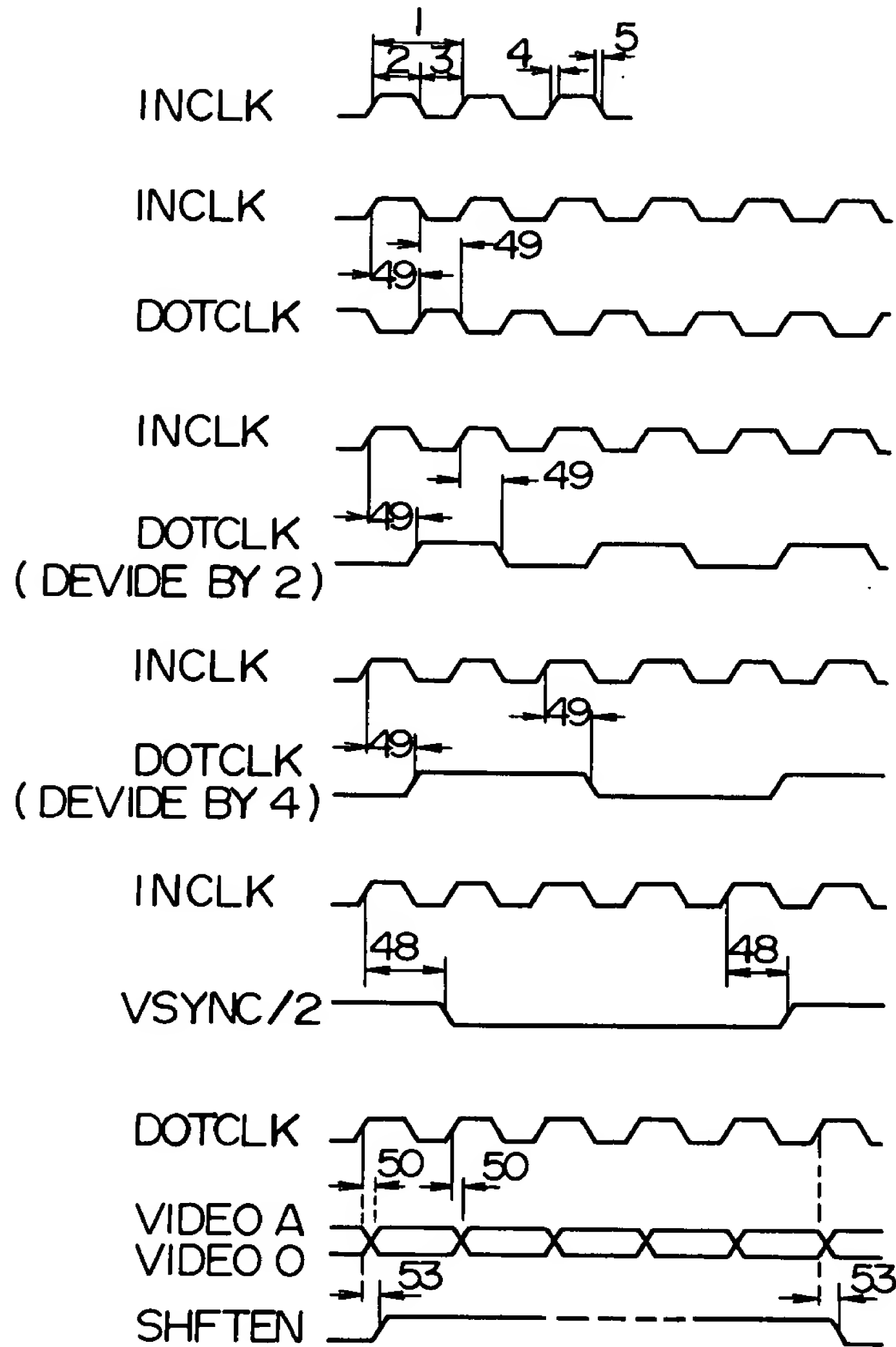
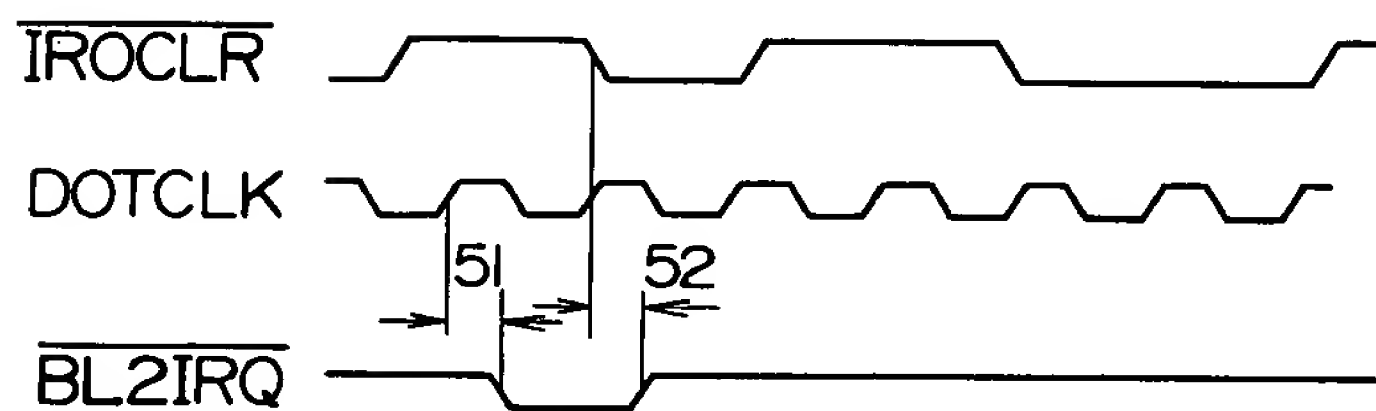


FIG. 26



O.G. FIG.	SUBCLASS
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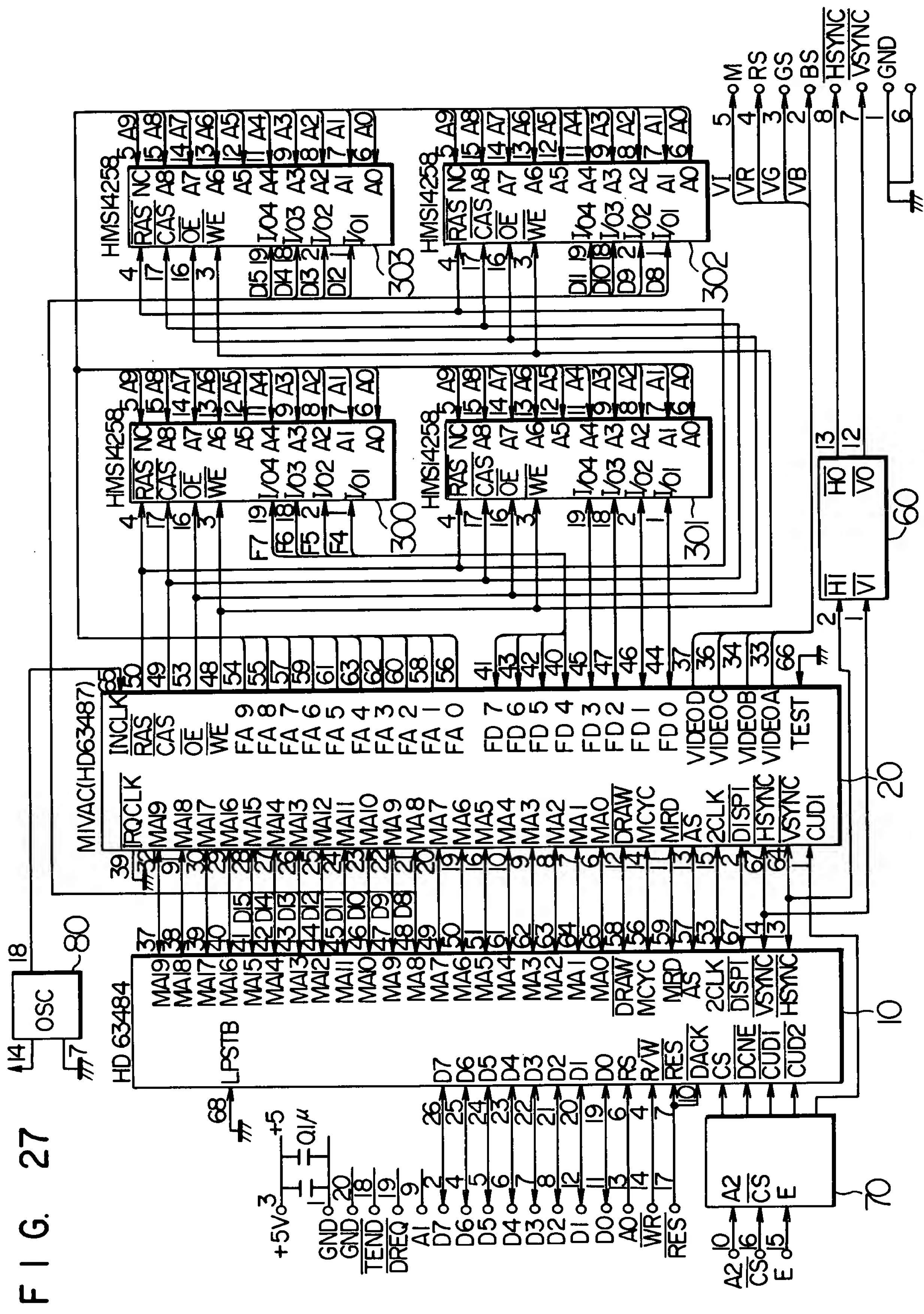


FIG. 28

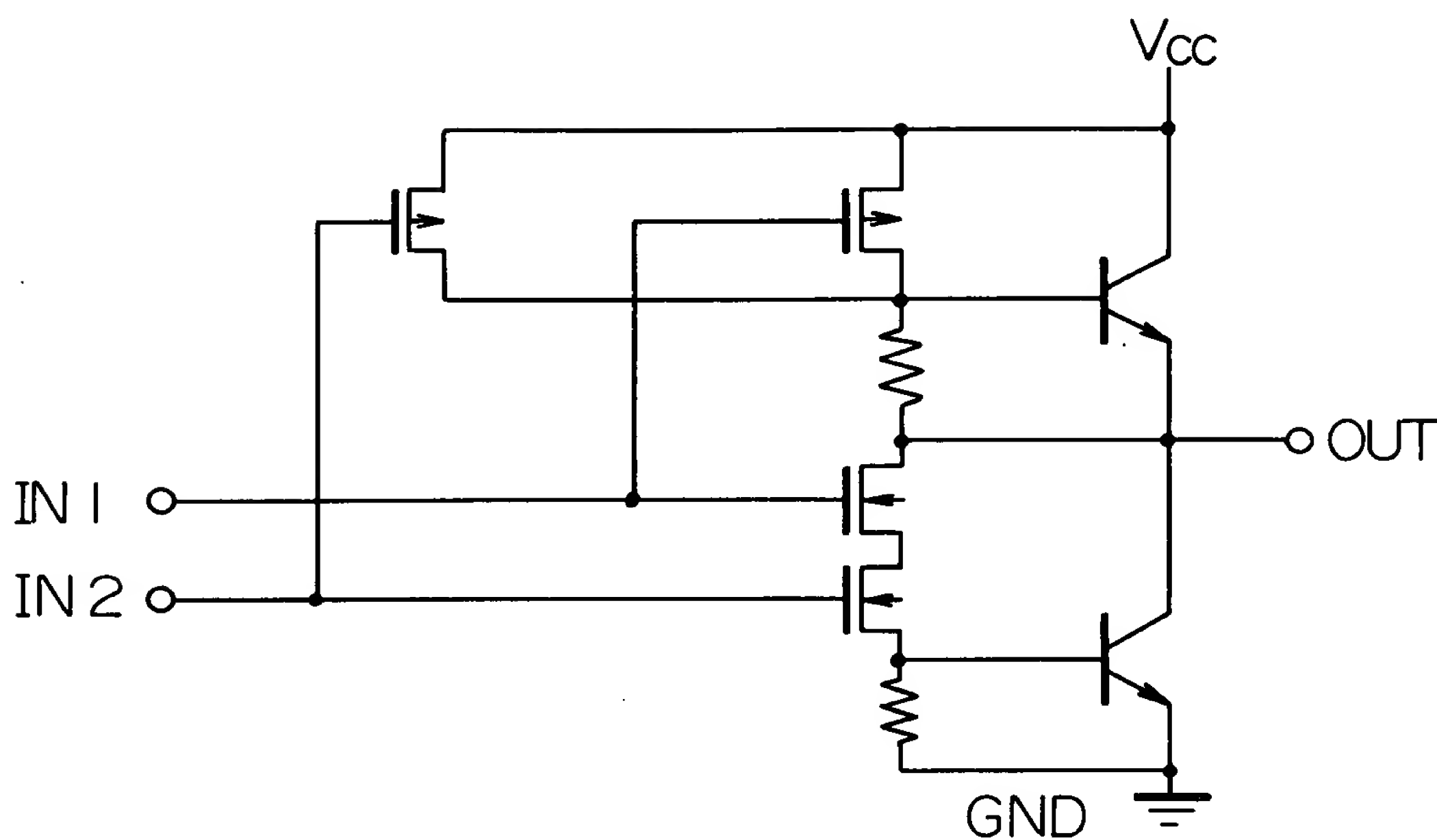


FIG. 29a

FA	4 ACCESSES / MCYC (DRAW , DISPLAY)				16 ACCESSES / 2 MCYCS (DISPLAY)			
	256Kx4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)		256Kx 4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)	
	ROM	COLUMN	ROM	COLUMN	ROM	COLUMN	ROM	COLUMN
9	—	—	MAD 8	NC0	—	—	MAD 8	NC0
8	MAD 9	NC1	MAD 9	NC1	MAD 9	NC1	MAD 9	NC1
7	MAD 8	NC2	MA 17	MAD 7	MAD 8	NC2	MA 17	MAD 7
6	MAD 7	MAD 6	MA 16	MAD 6	MAD 7	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	WC1	MAD 11	WC1
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	WC0	MAD 10	WC0

[] : COLUMN ADDRESS COUNTER

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APPROVED	O.G. FIG.	
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F I G. 29b

FA	2 ACCESSES / MCYC (DRAW)				4 ACCESSES / MCYC (DISPLAY)				16 ACCESSES / 2MCYCS (DISPLAY)			
	256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)		256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)		256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)	
	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	-	-	MA 18	[NCO]	-	-	MA 18	[NCO]	-	-	MA 18	[NCO]
8	MAD 9	[NCI]	MAD 9	MAD 8	MAD 9	[NCI]	MAD 9	MAD 8	MAD 9	[NC 1]	MAD 9	MAD 8
7	MAD 8	MAD 7	MA 17	MAD 7	MAD 8	MAD 7	MA 17	MAD 7	MAD 8	MAD 7	MA 17	MAD 7
6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	[WC 2]	MAD 12	[WC 2]
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	[WC 1]	MAD 11	[WC 1]
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	[WCO]	MAD 10	[WCO]	MAD 10	[WCO]	MAD 10	[WCO]

[] : COLUMN ADDRESS COUNTER

F I G. 29c

APPROVED	O.G. FIG.	
	CLASS	SUBCLASS
BY	DRAFTSMAN	

FA	1 ACCESSSES / MCYC (DRAW)				4 ACCESSSES / MCYC (DISPLAY)			
	256K x 4 -BIT (VMDO = 0)		1M x 4 -BIT (VMDO = 1)		256K x 4 -BIT (VMDO = 0)		1M x 4 -BIT (VMDO = 1)	
	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	—	—	MA 18	MAD 9	—	—	MA 18	MAD 9
8	MAD 9	MAD 8	MA 19	MAD 8	MAD 9	MAD 8	MA 19	MAD 8
7	MA 17	MAD 7	MA 17	MAD 7	MA 17	MAD 7	MAD 17	MAD 7
6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	WC1	MAD 11	WC1
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	WCO	MAD 10	WCO

□ □ : COLUMN ADDRESS COUNTER